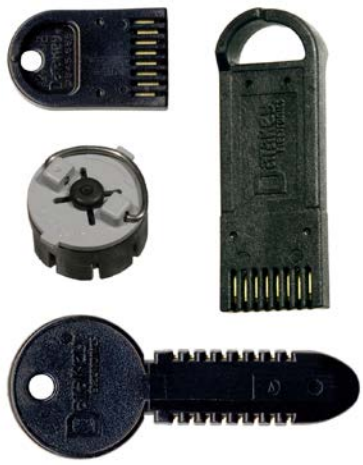
Datakey®

The power of memory. Secured.

MICROWIRE INTERFACE SPECIFICATION



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Notices and other considerations

Important notices

- Datakey guarantees the quality of its devices by testing each device prior to shipment. However, installing and using Datakey products is the responsibility of the purchaser and is in no way guaranteed by Datakey.
- Timing data, electrical characteristics and signal descriptions are based on a compilation of several approved manufacturer specifications. Datakey reviews the specifications of all approved vendors and "de-rates" the specifications as necessary to ensure that all devices meet our published specifications regardless of the vendor used. Customers must design to our published specifications to ensure that all devices operate correctly within an application. Designing to a particular vendor's specification is not recommended.
- Design Recommendation: It is recommended that all new key/token implementations be designed to operate with power supplies in the range of 2.7 to 3.6 volts. Although there is no immediate or certain future difficulties in the procurement of memory devices that operate with V_{cc} in the 4.5 to 5.5 volt range, it is possible the future availability of such memories may be impacted as semiconductor manufacturers continue to shrink their die geometries. Please contact the factory if you have any questions pertaining to this with your current or legacy design.
- While the information in this specification has been carefully reviewed, Datakey assumes no liability for any errors or omissions in this specification. Additionally, Datakey reserves the right to make changes to any part of the information in this specification or the products described herein without further notice.
- No part of this specification may be photocopied, reproduced or translated to another language without the prior written consent of Datakey.

Other considerations

- Although portable memory devices are designed to withstand harsh environments, many of the conditions that prevent them from functioning properly in such environments are best addressed through proper design of system interface circuits.
- Datakey tests all keys and tokens during the manufacturing process. In some cases, data written to a memory device remains after the test. Users should not rely on this data as a means of identifying keys or tokens.

Introduction

General description

Datakey portable memory keys and tokens contain electrically erasable programmable memory (EEPROM) accessed through a serial bus interface, using the Microwire, I²C, or SPI bus protocol. Each protocol controls input and output pins of the device through separate serial interface formats.

Portable memory device uses

Portable memory devices add functional versatility to many applications. They personalize equipment operations and transfer data in applications such as:

- Access control devices
- Instrument calibration equipment
- Fuel dispensers
- Medical treatment systems

Memory device design criteria

Portable memory applications require memory devices that can survive outside traditional environments, while maintaining data integrity when inserted and removed from the hosts that power them. Therefore, all portable memory devices must comply with the following basic design criteria:

- Resist dirt and other contaminants
- Transfer data reliably
- Tolerate electrostatic discharge
- Retain data when power is removed
- Retain data when exposed to certain environmental hazards

Manufacturers' design responsibility

Portable memory device manufacturers must address the above basic design criteria because they must develop memory devices capable of surviving in harsh environments. When a memory device is integrated into a larger system, other design considerations become important such as:

- How to dissipate electrostatic discharge (ESD)
- How to maintain device data integrity
- How to prevent host system disruption when inserting and removing the memory device

Continued on next page

Introduction, continued

Datakey portable memory devices

Datakey designs and manufactures portable, rugged keys and tokens containing non-volatile memory. Since 1976 our tough, reliable, re-programmable keys, tokens, receptacles and systems have solved data transport and access control problems in the most extreme environments.

Our Microwire keys and tokens contain serial EEPROMs accessed through a simple four-wire serial interface. Seven simple instructions control data transfers to and from the Microwire serial EEPROM. The Read command is used to access data stored in the device. Write and Write All commands store data in the device. Erase and Erase All commands are used to erase data from a device.

Data integrity is enhanced using the Erase/Write Enable and Erase/Write Disable instructions. These commands are used to enable or disable the ability to overwrite data stored in the device. Correct use of these commands reduces the potential for data corruption. All Microwire serial EEPROM devices power up with the Erase and Write instructions disabled.

What's in this specification

The remaining pages in this specification discuss Microwire design criteria for portable memory devices and recommend ways to handle them in typical applications.

Functional description

Keys and Tokens

The following are examples of serial EEPROM devices available from Datakey.

Each type of key and token is easily mated to a custom receptacle that provides access to the Microwire communication, power and ground signals described below.

LCK LCS LCX KSD

Signals

Table 1 shows descriptions of the signals for KC4210, SR4210 and KSD receptacles. Communication between the microcontroller and devices on a Microwire bus uses four signals: an active high chip select (CS), a clock (SK), a data in (DI) and a data out (DO). These signals, along with the voltage supply (Vcc) and ground signals are present on all keys and tokens. Table 1 shows signal acronyms and descriptions for the signals, followed by an explanation of each signal.

Table 1: Signal Acronyms and Descriptions

Signal Acronym	Signal Description
CS	Chip Select Input
DI	Serial Data Input
DO	Serial Data Output
SK	Serial Clock
Vcc	Supply Voltage
GND	Ground

Chip select (CS)

The chip select signal is an active high input to the device. A high level selects the device. A low level deselects the device and forces standby mode. However, an in-process programming cycle will be completed regardless of the CS input signal. If CS is driven low during a program cycle, the device will enter standby mode as soon as the programming cycle is completed. The CS signal must be low for a minimum period of time specified by the t_{CSL} between consecutive instructions. When the CS is low, the internal control logic is held in a RESET status and all signal activity on SK, DI and DO lines is ignored.

Continued on next page

Functional description, continued

Data in (DI)	The serial data in (DI) signal is an input to the device. Information such as the start bit, opcode, address and data bits is clocked into the device synchronously with the clock (SK) input signal via the DI signal. Data latches in on the rising edge of the clock signal.
Data out (DO)	The serial data out (DO) signal is an output from the device. DO is used in read mode to output data synchronously with the clock signal. It also provides READY/BUSY status information during erase and write cycles. READY/BUSY status information is available when the CS signal is high.
Serial clock (SK)	The serial clock is used to synchronize the communication between the master device and the memory chip. Opcode, address and data bits are clocked in on the rising edge of the SK signal. Data bits are clocked out on the rising edge of the SK signal. You can stop the SK signal anywhere in the transmission sequence *(at HIGH or LOW level)* and it can be continued anytime with respect to clock HIGH or clock LOW time. This gives the controlling master freedom to prepare the opcode, address and data.
Supply voltage (Vcc)	Two versions of keys and tokens are available: 5 Vdc nominal supply and 3.3 Vdc nominal supply. (See note at the beginning of the "Electrical Interface" Section.) **The Vcc signal must be controlled so that keys and tokens are not inserted into "live" receptacles. See section entitled "Memory Device Power and Signal Control".**
Ground (GND)	The ground signal and the system ground signal are common.

Instructions

Read and write operations

Microwire device read and write operations use seven instructions: Read, Write, Erase, Erase/Write Enable, Erase/Write Disable, Erase All and Write All. The format of each is presented in Tables 2 thru 4. Detailed information on each instruction and timing diagrams follow the tables.

Instruction sets

The serial commands for all Microwire keys and tokens differ only in length of address required: 1,024 bits, 4,096 bits and 16,384 bits. Tables 2 thru 4 show the instruction sets.

Table 2: 1,024 Bit Capacity *(64 x 16 bit Addresses)*

Instr	Start Bit	Opcode	Address	Data	Comment
Read	1	10	$A_5 – A_0$		Read memory location
Write	1	01	$A_5 – A_0$	$D_{15} – D_0$	Write memory location
WRAL	1	00	01 XXXX*	$D_{15} – D_0$	Write all memory with same data
ERAL	1	00	10 XXXX*		Erase all memory
Erase	1	11	$A_5 – A_0$		Erase memory location
EWEN	1	00	11 XXXX*		Erase/Write Enable
EWDS	1	00	00 XXXX*		Erase/Write Disable

X address bits must be clocked in; however, the values are DON'T CARE bits.

Table 3: 4,096 Bit Capacity *(256 x 16 bit Addresses)*

Instr	Start Bit	Opcode	Address	Data	Comment
Read	1	10	$A_7 – A_0$		Read memory location
Write	1	01	$A_7 – A_0$	$D_{15} – D_0$	Write memory location
WRAL	1	00	01 XXXXXX*	$D_{15} – D_0$	Write all memory with same data
ERAL	1	00	10 XXXXXX*		Erase all memory
Erase	1	11	$A_7 – A_0$		Erase memory location
EWEN	1	00	11 XXXXXX*		Erase/Write Enable
EWDS	1	00	00 XXXXXX*		Erase/Write Disable

***** *X address bits must be clocked in; however, the values are DON'T CARE bits.***

Continued on next page

Instructions, continued

Table 4: 16,384 Bit Capacity *(1024 x 16 bit Addresses)*

Instr	Start Bit	Opcode	Address	Data	Comment
Read	1	10	$A_9 - A_0$		Read memory location
Write	1	01	$A_9 - A_0$	$D_{15} - D_0$	Write memory location
WRAL	1	00	01 XXXXXXXX*	$D_{15} - D_0$	Write all memory with same data
ERAL	1	00	10 XXXXXXXX*		Erase all memory
Erase	1	11	$A_9 - A_0$		Erase memory location
EWEN	1	00	11 XXXXXXXX*		Erase/Write Enable
EWDS	1	00	00 XXXXXXXX*		Erase/Write Disable

X address bits must be clocked in, however, the values are DON'T CARE bits.

Instruction format

Each instruction follows the same basic format and contains the following information:

Bit	Description
Start bit	The start bit is the first logical '1' bit clocked into the device following an active Chip Select (CS) signal. Note that any number of '0' bits may be clocked in before a '1' bit.
Opcode bits	The opcode bits follow the start bit. The opcode specifies the instruction to execute. The opcode consists of two bits as shown in Tables 2 thru 4. Some instructions require the first two bits of the address field to completely specify the instruction.
Address bits	Address bits follow the opcode bits. The number of address bits clocked in depends on the capacity of the device being addressed. The correct number of bits for each device is shown in Tables 2 thru 4. As described previously, some instructions use the first two bits of the address field. For those instructions, it is still necessary to clock in the correct number of address bits *(including the first two bits*) for the device being addressed; however, the bits are DON'T CARE values.
Data bits	The data bits for instructions with a data field associated with them *(Read, Write and Write All)* follow the address bit field. In the case of a Write or Write All instruction, the data bits are clocked in on the Data In (DI) signal.

Microwire device read and write cycles

Read cycles

The Read instruction outputs the data stored at an addressed memory location on the data output (DO) pin. After the device receives a Read instruction, the instruction and address are decoded.

Data transfers from the memory register into a 16-bit serial shift register. A dummy bit *(logical "0")* precedes the 16-bit output string. Output of the dummy bit is triggered by the rising edge of the clock for the last address bit. The output data changes during the rising edge of the system clock. Once the 16-bit output data string is read, the chip select line (CS) is driven low to end the read cycle.

The internal address pointer is incremented after the last data bit is read. Sequential data reads may be performed provided the CS line remains high. During a data output from the next address location, there is no dummy bit. See Figure 1.

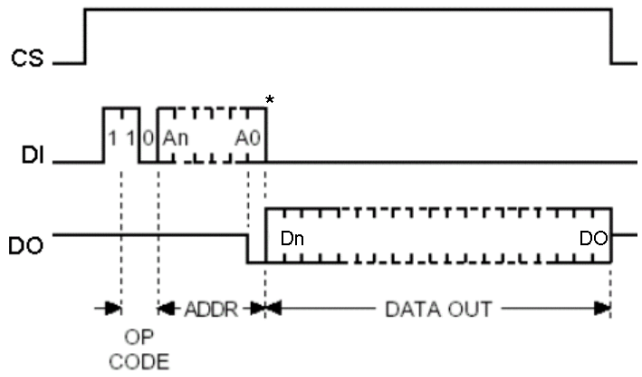

Figure 1: Read Cycle Timing Chart

**See Tables 2 thru 4 to determine the number of address bits or DON'T CARE bits that must be clocked into the selected device.*

Note: Sequential read operations are not guaranteed for Keys and Tokens manufactured before August, 2004.

Continued on next page

Microwire device read and write cycles, continued

Erase/Write Enable/Disable

When power is applied to a Key or Token, the device enters the "programming disabled" state; therefore, an Erase/Write Enable (EWEN) command must precede the Write or Erase instruction. Once the EWEN instruction has been issued, the next Erase and Write instructions will be valid until an Erase/Write Disable (EWDS) instruction is sent to the device. Read instructions are not affected by the programming state of the device. See Figures 2 and 3 for an illustration of the EWEN and EWDS instructions.

Note: It is recommended that the EWEN instruction be sent only before the programming operation, and that you issue the EWDS instruction following a programming operation. This sequence helps prevent accidental programming due to noise or inadvertent writes.

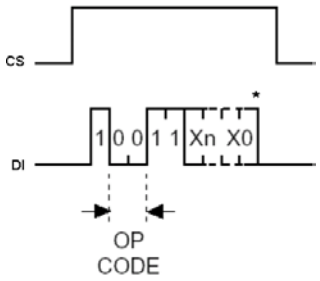

Figure 2: Erase/Write Enable

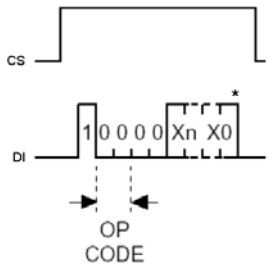

Figure 3: Erase/Write Disable

**See Tables 2 thru 4 to determine the number of address bits or DON'T CARE bits that must be clocked into the selected device.*

Continued on next page

Microwire device read and write cycles, continued

Write cycle

A Write instruction programs the 16 bits of data that follow the instruction opcode and address bits into the specified address. Once the Data In (DI) pin receives the last data bit, the Chip Signal (CS) is driven low before the next rising edge of the Serial Clock (SK) signal. The falling edge of CS signal initiates the self-timed write programming cycle.

The DO pin indicates the status of the programming cycle if the CS input is driven high after a minimum time specified by t_{CSL}. The Data Out (DO) pin will be tri-stated before the self-timed write cycle starts. When the DO pin is low, programming is in progress. When the DO pin is high, the data pattern specified in the instruction is in the designated memory address and the device is ready for another instruction. The DO pin will return to a tri-state level when the CS signal is driven low. It is not necessary to provide an SK signal while monitoring the status of the DO pin. See Figure 4.

Note: An Erase/Write Enable instruction must be issued to the device before sending a Write instruction. It is recommended that an Erase/Write Disable instruction be issued following the Write instruction.

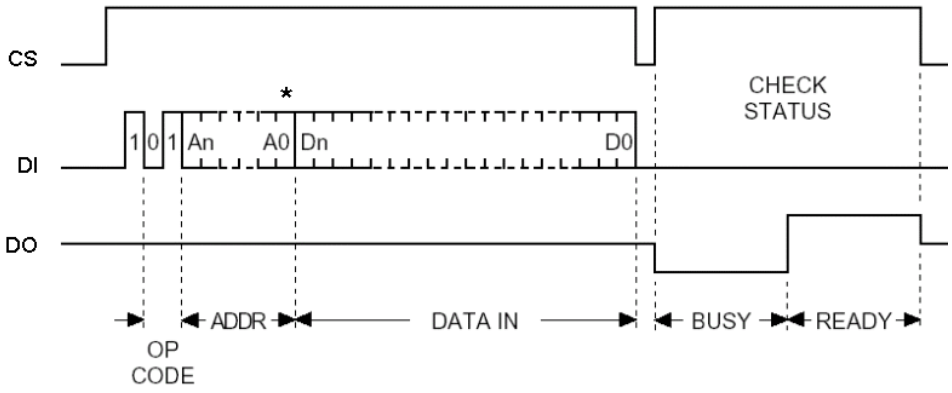

Figure 4: Write Cycle Timing Chart

**See Tables 2 thru 4 to determine the number of address bits or DON'T CARE bits that must be clocked into the selected device.*

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Microwire device read and write cycles, continued

Erase cycle

The Erase instruction forces all data bits at the specified address to a logical "1" state. Once the instruction opcode and address bits are clocked in, the CS line is driven low before the next rising edge of the serial clock (SK). The falling edge of the CS initiates the self-timed erase cycle. If the CS signal is then driven high *(after observing the minimum time specified by t_{CSL})*, the DO pin will show the status of the chip as (READY/BUSY). If the erase cycle is still in progress, the DO pin will be low. It will go high after the erase cycle completes, and the device is ready for the next instruction. The DO signal will return to a tri-state status when the CS signal is driven low.

It is not necessary to provide an SK signal while monitoring the status of the DO pin. See Figure 5.

Note: An Erase/Write Enable instruction must be issued to the device before sending an Erase instruction. It is recommended that an Erase/Write Disable instruction be issued following the Erase instruction.

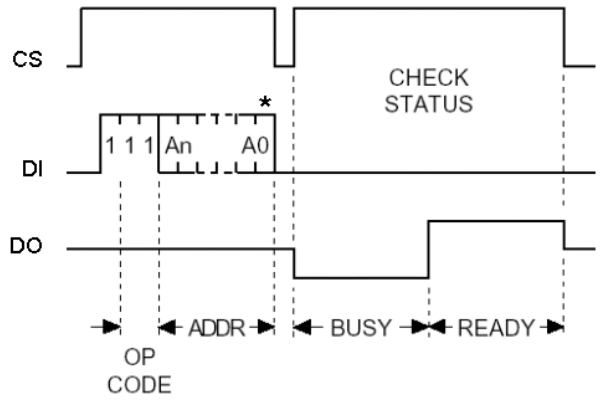

Figure 5: Erase Cycle Timing Chart

**See Tables 2 thru 4 to determine the number of address bits or DON'T CARE bits that must be clocked into the selected device.*

Continued on next page

Microwire device read and write cycles, continued

Erase All

An Erase All (ERAL) instruction will erase the entire memory array to the logical "1" state. The chip erase timing cycle is identical to the erase cycle. See Figure 6.

Notes:

1. The Erase All (ERAL) instruction is not supported in devices that operate with a supply voltage less than 4.5 volts.
2. An Erase/Write Enable instruction must be issued to the device before sending an Erase instruction. It is recommended that an Erase/Write Disable instruction be issued following the Erase All instruction.

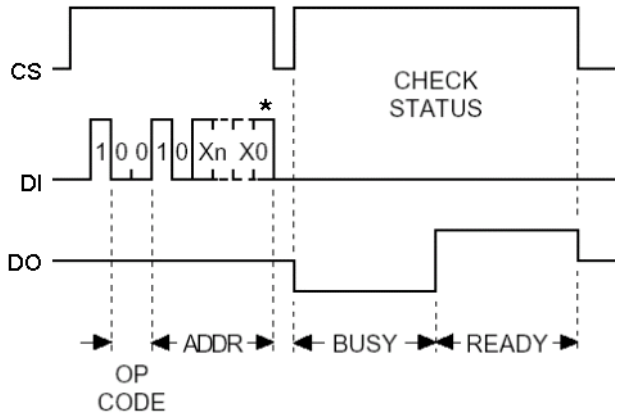

Figure 6: Erase All Timing Cycle Chart

**See Tables 2 thru 4 to determine the number of address bits or DON'T CARE bits that must be clocked into the selected device.*

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Microwire device read and write cycles, continued

Write All

A Write All (WRAL) instruction will write the entire memory array with the data specified in the command. The WRAL instruction timing is similar to the Write instruction timing. See Figure 7.

Notes:

1. The Write All (WRAL) instruction is not supported for devices that operate with a supply voltage of less than 4.5 volts.
2. An Erase/Write Enable instruction must be issued to the device before sending a Write instruction. It is recommended that an Erase/Write Disable instruction be issued following the Write All instruction.

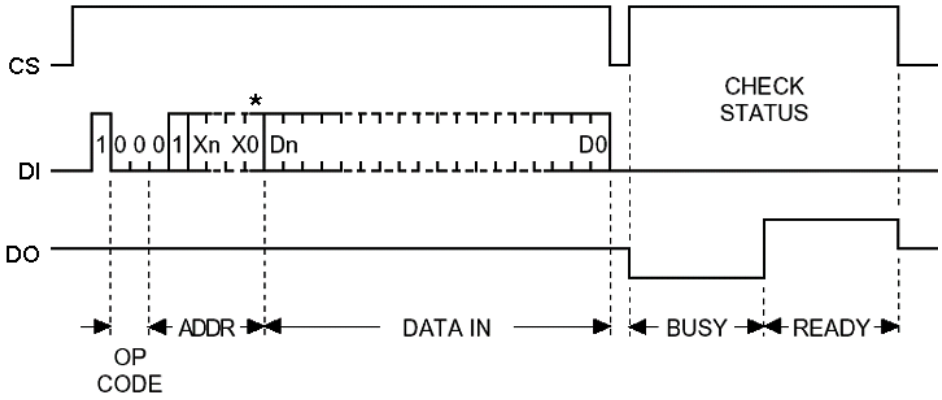

Figure 7: Write All Timing Cycle Chart

**See Tables 2 thru 4 to determine the number of address bits or DON'T CARE bits that must be clocked into the selected device.*

Panel- and board-mount receptacle descriptions

Receptacles

The receptacles are used to interface the host system directly with specific serial data keys and tokens. The styles are the KC4210, KC4210PCB, SR4210, SR4210PCB and the KSD.

A Last On/First Off (LOFO) switch in the key or token receptacle enables the host system to determine when a key or token is present. Upon insertion of a key or token, the LOFO contact connects to ground. Conversely, when the key is removed, the LOFO contact is open. The LOFO contact allows system designers to detect the presence of a key or token, and protect the host bus by applying power only when a key or token is fully inserted into the receptacle.

KC4210 Panel-Mount receptacle

The KC4210 panel-mount version is designed for applications that require easy mounting in a front panel configuration. To mount the device, simply cut a 1-inch square hole in the desired panel location and snap the receptacle into place. A standard 10-pin connector cable (5 x 2) is used to connect the device to your host. See Figure 8.

Figure 8: Panel-Mount KC4210 Receptacle

Note: It is recommended that the total length of signal conductors, PC board traces and ribbon cables not exceed 8 inches.

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Panel- and board-mount reeceptacle descriptions, continued

KC4210 orthographic drawing

Figure 9 shows the KC4210 panel-mount receptacle. Refer to spec sheet for dimensions.

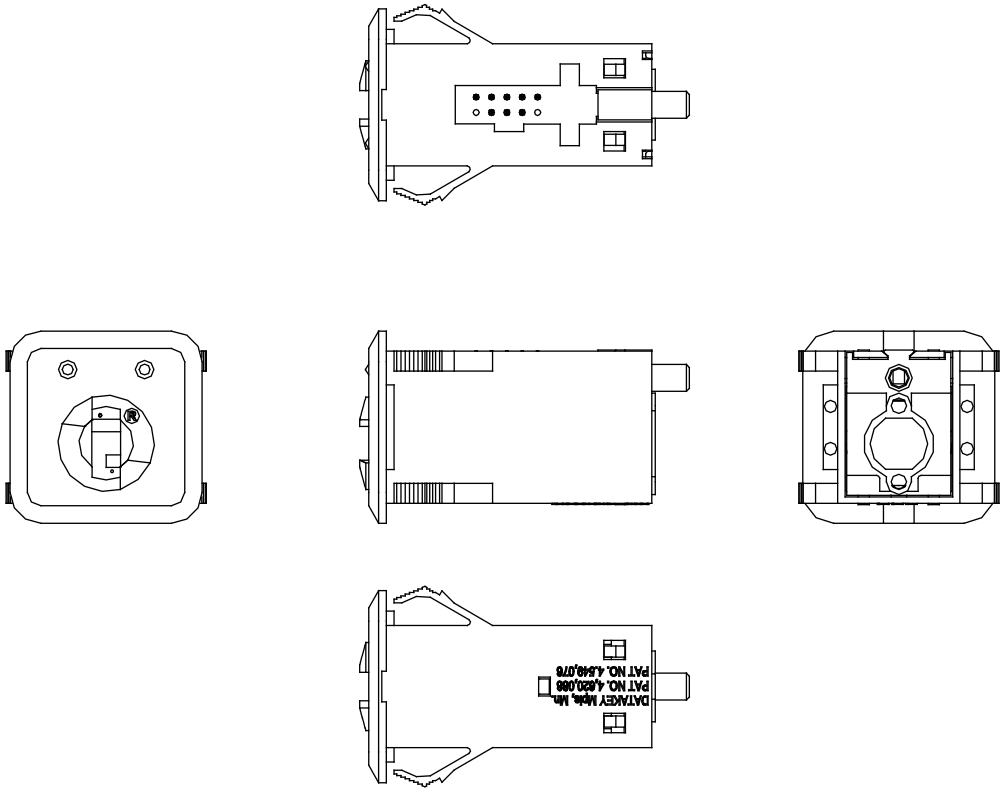

Figure 9: KC4210 Receptacle Physical Orthographic Drawing

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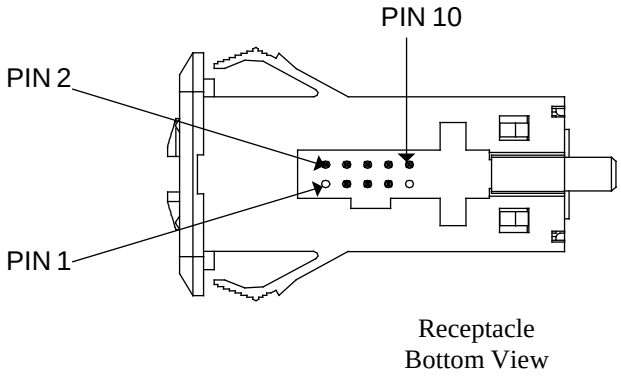
Panel- and board-mount receptacle descriptions, continued

KC4210 pin outs See Figure 10 KC4210 receptacle pin outs.



Microwire	
Pin No.	**Description**
Pin 1	NC
Pin 2	Power (Vcc)
Pin 3	Ground (Vss)
Pin 4	NC
Pin 5	Chip Select (CS)
Pin 6	Data In (DI)
Pin 7	Serial Clock (SK)
Pin 8	Data Out (DO)
Pin 9	NC
Pin 10	LOFO

Figure 10: KC4210 Receptacle Pin Outs

Continued on next page

Panel- and board-mount receptacle descriptions, continued

KC4210PCB board-mount receptacle

The board-mount version is designed for applications where the designer wants to mount the device directly onto a printed circuit board. In such applications, the key receptacle connects to the host by soldering the leads onto a printed circuit board. See Figure 11.

Figure 11: KC4210PCB Board-Mount Receptacle

KC4210PCB orthographic drawing

Figure 12 shows the KC4210PCB board-mount receptacle. Refer to spec sheet for dimensions.

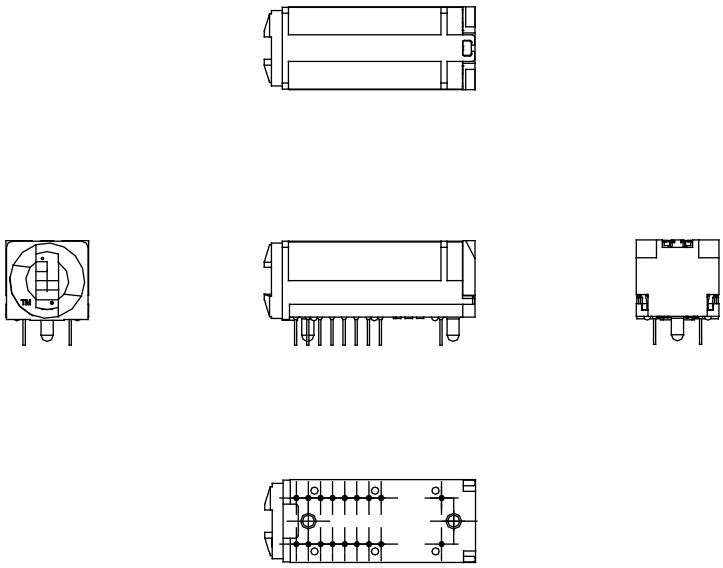


Figure 12: KC4210PCB Receptacle Dimensions

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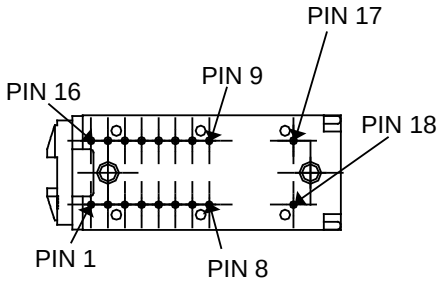
Panel- and board-mount receptacle descriptions, continued

KC4210PCB pin outs

See Figure 13 for receptacle pin outs.



Microwire	
Pin No.	**Description**
Pin 1	NC
Pin 2	Ground (Vss)
Pin 3	Power (Vcc)
Pin 4	NC
Pin 5	Data Out (DO)
Pin 6	Chip Select (CS)
Pin 7	Serial Clock (SK)
Pin 8	Data In (DI)
Pin 9	Data In (DI)
Pin 10	Serial Clock (SK)
Pin 11	Chip Select (CS)
Pin 12	Data Out (DO)
Pin 13	NC
Pin 14	Power (Vcc)
Pin 15	Ground (Vss)
Pin 16	NC
Pin 17	LOFO
Pin 18	LOFO

Figure 13: KC4210PCB Receptacle Pin Outs

KC4210 key styles

The KC4210 panel- and board-mount receptacles accept two key styles. The DK and the LCK come in memory sizes from 1 to 16 Kb. See Figure 14.

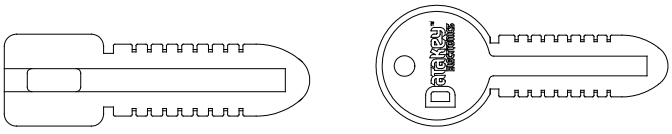


Figure 14: DK and LCK Keys for KC4210 Receptacle

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Panel- and board-mount receptacle descriptions, continued

SR4210 panel mount receptacle

The SR4210 panel-mount version is designed for applications that require easy mounting in a front-panel configuration. To mount the SR4210 panel-mount receptacle, simply cut a hole based on the dimensions shown on the SR4210 spec sheet in the desired panel location and then slip it into place. A standard 10-pin connector cable *(5 x 2)* is used to connect the device to the host. A Last On/First Off (LOFO) switch in the Receptacle enables the host system to determine when a token is present. See Figure 15.

Figure 15: SR4210 Panel-Mount Receptacle and Clip

Note: It is recommended that the total length of signal conductors, PC board traces and ribbon cables not exceed 8 inches.

SR4210 orthographic drawing

Figure 16 shows the SR4210 panel mount receptacle. Refer to spec sheet for dimensions.

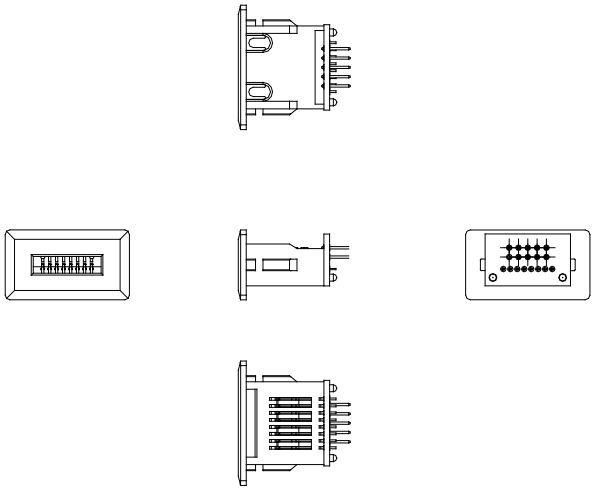

Figure 16: SR4210 Receptacle Orthographic Drawing

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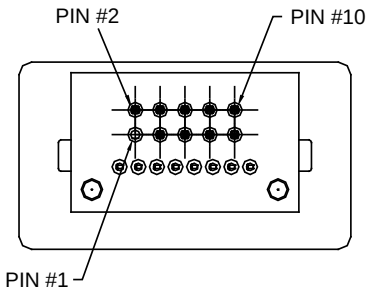
Panel- and board-mount receptacle descriptions, continued

SR4210 pin outs

See Figure 17 for receptacle pin outs.



Microwire	
Pin	**Description**
Pin 1	NC
Pin 2	Power (Vcc)
Pin 3	Ground (Vss)
Pin 4	NC
Pin 5	Chip Select (CS)
Pin 6	Data In (DI)
Pin 7	Serial Clock (SK)
Pin 8	Data Out (DO)
Pin 9	NC
Pin 10	LOFO

Figure 17: SR4210 Receptacle Pin Outs

Continued on next page

Panel- and board-mount receptacle descriptions, continued

SR42XXPCB mount receptacles

The information on the SR4210PCB below also applies to the SR4220, SR4230 board-mount receptacles. Dimensions can be found in the corresponding spec sheets. Contact the factory for information on SMT options.

SR4210PCB board-mount receptacle

The SR4210PCB board-mount receptacle is designed for applications where the designer wants to mount the device directly onto a printed circuit board. In such applications, the receptacle connects to the host by soldering the leads onto a printed circuit board. See Figure 18.

Figure 18: SR4210PCB Mount Receptacle

SR4210PCB orthographic drawing

Figure 19 shows the SR4210PCB board-mount receptacle. Refer to spec sheet for dimensions.

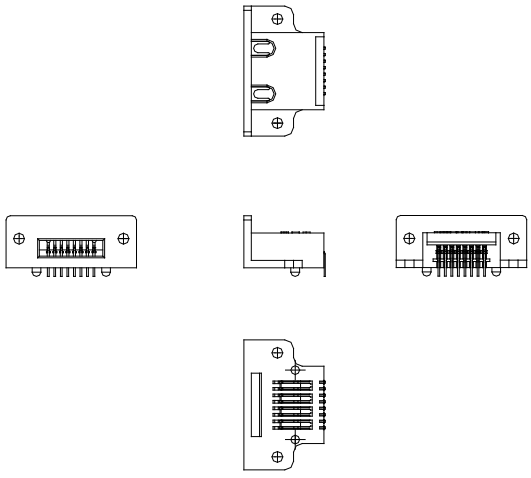


Figure 19: SR4210PCB Board-Mount Receptacle Dimensions

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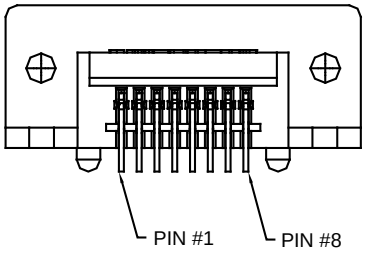
Panel- and board-mount receptacle descriptions, continued

SR4210PCB pin outs

See Figure 20 for SR4210PCB receptacle pin outs.

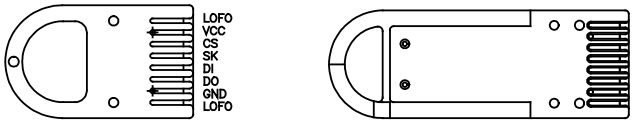


Microwire	
Pin	**Description**
Pin 1	LOFO
Pin 2	Power (Vcc)
Pin 3	Chip Select (CS)
Pin 4	Serial Clock (SK)
Pin 5	Data In (DI)
Pin 6	Data Out (DO)
Pin 7	Ground (Vss)
Pin 8	LOFO

Figure 20: SR4210PCB Pin Outs

Slim token styles

The SR4210 panel- and PCB-mount receptacles accept the IST- and ISX-Token style with memory sizes from 1Kb to 512Kb. Figure 21 shows the token styles and pinout.



LCS **LCX**

Figure 21: LCS and LCX Token Styles for SR4210 Receptacles

Continued on next page

Panel- and board-mount receptacle descriptions, continued

KSD receptacle

The KSD receptacle accepts KSD Plugs. It can be used in board- and panel-mount applications. Figure 22 and 23 show pictures of the KSD receptacle and KSD Plug.

Figure 22: KSD Receptacle

Figure 23: KSD Plug

KSD receptacle orthographic drawing

Figure 24 shows a bottom view of a KSD receptacle diagram and a description of its pin outs when used with an KSD Plug.

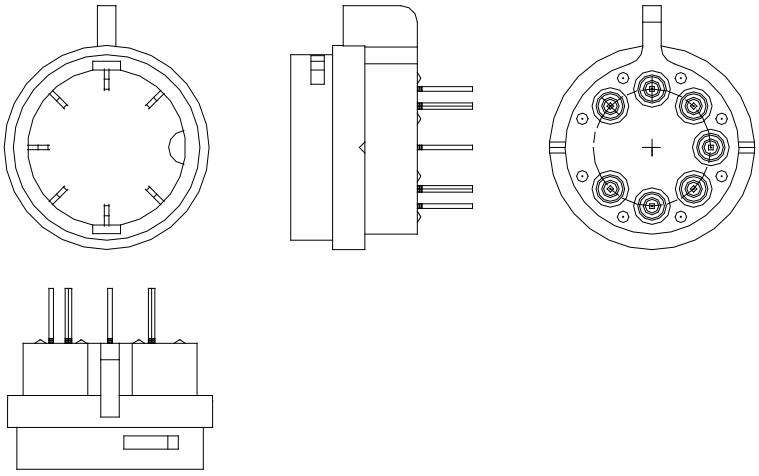


Figure 24: KSD Receptacle Orthographic Drawing

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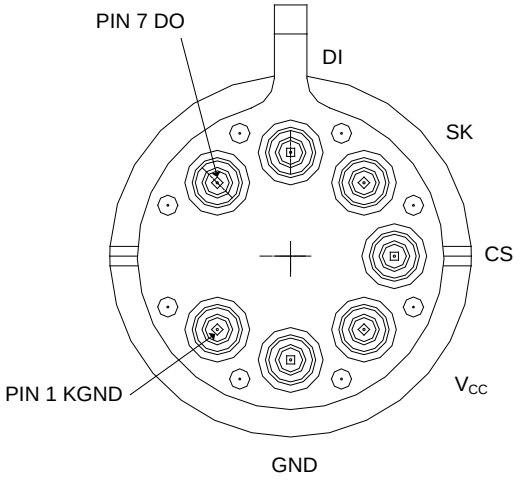
Panel- and board-mount receptacle descriptions, continued

KSD pin outs See 25 for KSD receptacle pin outs.



Microwire	
Pin	**Description**
Pin 1	KGND*
Pin 2	Ground
Pin 3	Power (VCC)
Pin 4	Chip Select (CS)
Pin 5	Serial Clock (SK)
Pin 6	Data In (DI)
Pin 7	Data Out (DO)

Note: KGND is connected to GND inside the plug. When a plug is inserted into the receptacle KGND is pulled “low”. The host monitors the KGND signal to determine the presence of the Plug.

Figure 25: KSD Receptacle Pin Outs

Electrical interface

AC/DC electrical characteristics

Tables 5 thru 9 show specific common DC and AC electrical characteristics for serial Microwire keys and tokens. Keys and tokens manufactured after August, 2004 were available in two nominal operating voltage ranges: 5.0 volts and 3.3 volts. Keys and tokens manufactured after May, 2006 have a wide operating voltage range of 2.7 to 5.5 volts. Tables 6 and 7 provide the electrical characteristics for these keys and tokens. **FOR KEYS AND TOKENS MANUFACTURED BEFORE AUGUST 2004, SEE TABLES 8 AND 9.**

Maximum specifications

Stressing Microwire keys and tokens beyond the limits specified in Table 5 could cause permanent damage to the device. The conditions indicated in Table 5 are stress ratings only. Exposure to absolute maximum stress levels for extended periods may affect device reliability. Operating levels are specified in Tables 6 thru 9.

Table 5: Absolute Maximum Values and Temperature

Symbol	Parameter	Min/Max	Units
V_{CC}	Supply voltage	6.5	V
$V_{IN/OUT}$	All pins w.r.t. Ground	-0.3 to 6.5	V
T_{STG}	Storage temperature	-65 to 150	°C
T_{BIAS}	Operating temperature[1]	-40 to 85	°C

[1] Keys and tokens manufactured before 2004 have an operating temperature range of 0 to 70 degrees C.

Design Recommendation: It is recommended that all new key/token implementations be designed to operate with power supplies in the range of 2.7 to 3.6 volts. Although there is no immediate or certain future difficulties in the procurement of memory devices that operate with V_{cc} in the 4.5 to 5.5 volt range, it is possible the future availability of such memories may be impacted as semiconductor manufacturers continue to shrink their die geometries. Please contact the factory if you have any questions pertaining to this with your current or legacy design.

Continued on next page

Electrical interface, continued

Table 6: DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Supply voltage[1]	2.7 3.0 4.5	5.5 3.6 5.5	V V V	Wide Voltage Range 3.3 V nominal 5.0 V nominal
V_{IH}	High level voltage input	0.7xVcc	Vcc + 1.0	V	
V_{IL}	Low level voltage input	-0.3	0.2xVcc	V	
V_{OL}	Low level voltage output		0.4	V	I_{OL} = 2.1 mA, Vcc = 4.5 V
V_{OH}	High level voltage output	2.4		V	I_{OL} = -400 µA, Vcc = 4.5 V
I_{LI}	Input leakage current		± 2.5	µA	V_{IN} = 0 to Vcc
I_{LO}	Output leakage current		± 2.5	µA	V_{IN} = 0 to Vcc, CS = 0
C_{IN}	Input pin capacitance		7.0	pF	V_{IN} = 0 V
C_{OUT}	Output pin capacitance		7.0	pF	V_{OUT} = 0 V
I_{CC}	Supply current		3.0	mA	CS = V_{IH}, SK = 1 MHz, Vcc = 5.0 V
I_{CCS}	Supply current standby		50.0	µA	Vcc = 5.0 V, CS = 0 V, SK = 0 V

[1] Microwire keys and tokens were formerly available in two nominal operating votagles: 5 VDC and 3.3 VDC.

Continued on next page

Electrical interface, continued

Table 7: AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{SK}	Clock frequency		1	MHz	
t_{SKH}	Clock high time[1]	350		ns	
t_{SKL}	Clock low time[1]	350		ns	
t_{SKS}	Clock setup time	100		ns	
t_{CSS}	Chip select setup time	100		ns	
t_{CSH}	Chip select hold time	0		ns	
t_{CSL}	Chip select low time[2]	1000		ns	
t_{CLSH}	Chip select low to clock high	250		ns	
t_{DIS}	Data in setup time	100		ns	
t_{DIH}	Data in hold time	100		ns	
t_{PD0}	Delay to output low		400	ns	C_L = 100pF
t_{PDV}	Delay to output valid		400	ns	C_L = 100pF
t_{SV}	Delay to status valid		400	ns	C_L = 100pF
t_{CZ}	Chip select low to output high Z		200	ns	
t_{WC}	Erase/write cycle time		15	ms	

Notes:

1. $t_{SKH} + t_{SKL} \geq 1/f_{SK}$
2. The chip select signal must be brought low for a minimum of t_{CSL} between consecutive instructions.

Continued on next page

Electrical interface, continued

IMPORTANT

Keys and tokens manufactured before August, 2004 are specified below. Note that these devices operate at a slower clock rate and within a narrower voltage range. If systems are developed or modified supporting old and new keys or tokens, it is required to design systems using the specifications listed in Tables 8 and 9.

Table 8: DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Supply voltage	4.75	5.25	V	
V_{IH}	High level voltage input	2.2	Vcc + 0.5	V	
V_{IL}	Low level voltage input	-0.1	0.8	V	
V_{OL}	Low level voltage output	--	0.4	V	I_{OL} = 2.1 mA, Vcc = 4.5 V
V_{OH}	High level voltage output	4.0	--	V	I_{OL} = -400 µA, Vcc = 4.5 V
I_{LI}	Input leakage current		± 100	µA	V_{IN} = 5.25
I_{LO}	Output leakage current		± 100	µA	V_{IN} = 5.25, CS = 0
C_{IN}	Input pin capacitance		7.0	pF	V_{IN} = 0 V
C_{OUT}	Output pin capacitance		7.0	pF	V_{OUT} = 0 V
I_{CC}	Supply current[1]		3.0	mA	CS = V_{IH}, SK = 125 KHz, Vcc = 5.25 V
I_{CCS}	Supply current standby		1.0	mA	Vcc = 5.0 V, CS = 0 V, SK = 0 V

[1] Peak operating current will be 10 mA maximum during a write all operation.

Continued on next page

Electrical interface, continued

IMPORTANT

Keys and tokens manufactured before August, 2004 are specified below. Note that these devices operate at a slower clock rate and within a narrower voltage range. If systems are developed or modified supporting old and new keys or tokens, it is required to design systems using the specifications listed in Tables 8 and 9.

Table 9: AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{SK}	Clock frequency	0.1	125	KHz	
t_{SKH}	Clock high time[1]	2000		ns	
t_{SKL}	Clock low time[1]	2000		ns	
t_{SKS}	Clock setup time	400		ns	
t_{CSS}	Chip select setup time	400		ns	
t_{CSH}	Chip select hold time	400		ns	
t_{CSL}	Chip select low time[2]	2000		ns	
t_{CLSH}	Chip select low to clock high	250		ns	
t_{DIS}	Data in setup time	700		ns	
t_{DIH}	Data in hold time	400		ns	
t_{PD0}	Delay to output low		3000	ns	C_L = 100pF
t_{PDV}	Delay to output valid		3000	ns	C_L = 100pF
t_{SV}	Delay to status valid		2000	ns	C_L = 100pF
t_{CZ}	Chip select low to output high Z		500	ns	
t_{WC}	Erase/write cycle time		15	ms	

Notes:

1. $t_{SKH} + t_{SKL} \geq 1/FSK$
2. The chip select signal must be driven low for a minimum of t_{CSL} between consecutive instructions.

Timing diagrams

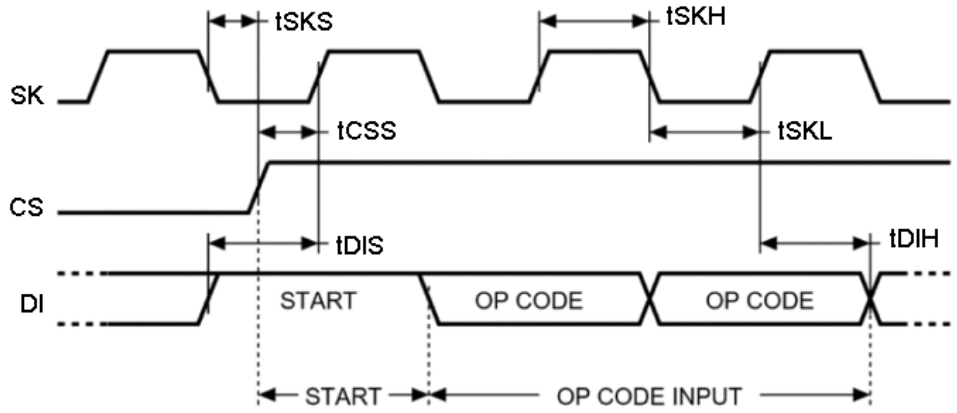


Figure 26: All Operations Timing

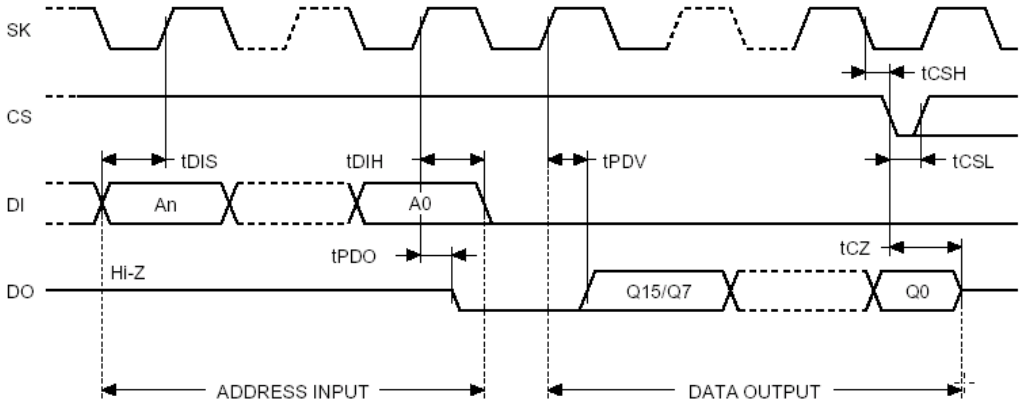


Figure 27: Read Operation Timing

Continued on next page

Timing diagrams, continued

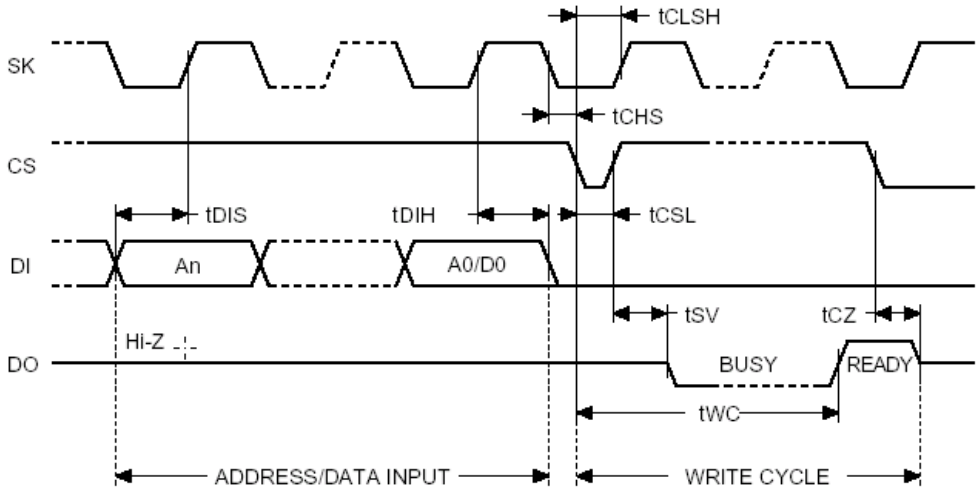


Figure 28: Erase, Write, Erase All, Write All Operations Timing

Electrostatic discharge (ESD)

Circuit component damage	A buildup of electrostatic charge gradients across the surface of a memory device can produce voltages that could damage circuit components. To prevent such damage, Datakey portable memory devices integrate materials, circuits and mechanical barriers that help to ensure uniform voltage across the circuit.
Electrostatic charge voltage levels	Any system that uses memory devices must also provide a means of dissipating electrostatic charges. By simply holding a portable memory device in your hand, it is possible to build up an electrostatic charge across the surface of the memory device up to 20KV relative to ground. This would be equivalent to connecting a circuit of several hundred picofarads of capacitance with a low-series resistance to the memory device.
Electrostatic charge dissipation	When you insert a portable memory device into a system that is grounded or at some other potential, the built-up charge from handling the memory device must be safely dissipated. This can be done by providing a path to ground for the charge. The path must be controlled to prevent large currents and high voltages from occurring on the memory device and in the receptacle. This can be done by putting a resistor in the circuit trace for the receptacle, and using over-voltage protection devices to direct the charge to system ground.

Memory device power and signal control

Poor contact concerns

When inserting a portable memory device into a receptacle, there can be poor contact between the memory device and receptacle. There can be several possible reasons for this:

Dirty contact surfaces: To make enough electrical contact, the contact surfaces must be free of contaminants. This requires that the contacts be cleaned through a wiping action from the portable memory device.

The contacts could bounce and require some time to settle. This could result in a series of random make and break conditions on any or all the contacts.

When a memory device is removed from a receptacle, the contacts do not always break evenly or cleanly.

Power concerns

When power is applied to a memory device when inserted or removed from a Receptacle, random contact makes and breaks could cause significant problems for the memory device and the receptacle. Because the control and address signals are not controlled during those actions, undesirable logic combinations could occur, such as:

Power and ground connections becoming unstable, causing further unpredictability.

Fast power switching to a memory device introducing noise into system power and ground distribution circuits, resulting in electrical damage to the memory device and corruption to its data.

Data corruption prevention

The integrated circuits used in Datakey memory devices are designed to reduce the risk of data corruption during transient conditions. For example, memory devices require a Write Enable command before storing any data. Write commands are also not permitted if the supply voltage is less than a prescribed value. As effective as these protection schemes might be, however, they do not always eliminate the potential problems with noise that could occur when power is applied to a circuit via a bouncing contact.

To avoid these problems, it is important to control the memory device's power and signal connections. This can be done by using detection circuits, which are discussed next.

Continued on next page

Memory device power and signal control, continued

Memory device detection circuit

This circuit detects when a memory device is present. Datakey receptacles use Last On/First Off (LOFO) contacts for this purpose. When inserting a memory device into the receptacle, the LOFO contacts make electrical connection only after all memory device contacts are closed. Similarly, the LOFO contacts break before any other contact is open.

Transistor switch circuit

When a receptacle detects a memory device for a certain minimum time, power can then be applied. This delay can be established by using a simple transistor switch circuit with the following characteristics:

The power switch should have a low voltage drop when power is applied to the memory device. This will ensure that the voltage supplied to the memory device is within its tolerance.

The circuit should apply power to any pull-up resistors connected to the memory device to prevent power from being applied unintentionally through the signal lines.

The circuit should include a bleeder resistor to ensure that power is removed quickly when the switch is turned off.

The switch should turn power on fast enough to avoid causing problems in the memory device, and slow enough so that it does not introduce any significant noise into the system-reset circuit.

Microwire read and write procedures

Procedures

Follow the procedures below when using a portable memory device in a receptacle with a power switching circuit.

Read procedure

The procedure for reading data from a memory device is less critical than the sequence for writing data to that same device because the data is not subject to change. To read the data from a memory device, Datakey recommends the following procedure:

Insert memory device

Detect a memory device using the LOFO contact

Wait for contacts to settle (verify memory device is still present)

Apply power

Wait for power to stabilize

Test contact integrity

Read data

Remove power

Remove memory device

Continued on next page

Microwire read and write procedures, continued

Write procedure

The write procedure must verify that the memory device is present throughout the write cycle; this will ensure that data is written to the memory device correctly. To write data to a memory device, Datakey recommends the following procedure:

Insert memory device

Detect a memory device using the LOFO contact

Wait for contacts to settle (verify memory device is still present)

Apply power

Wait for power to stabilize

Test contact integrity

Write data

Verify memory device is still present *(if not, indicate an error)*

Verify the data written (if appropriate, indicate an error)

Remove power

Remove memory device

Long read/write operation

Large capacity memory systems should also be protected against memory device removal during long read or write operations. An activity light could be all that is needed for some applications. Other installations could require physical barriers or interlocks to ensure that the memory device being read or written to remains in place.

Acknowledgement

ST Microelectronics Timing diagrams courtesy of ST Microelectronics, reprinted by permission.

Revision History

Date	Revision	Description
01/03	A	Initial issue of Microwire interface specification.
07/04	B	Microwire instruction tables revised and added as errata sheet.
10/04	C	Added revised instruction tables and other modifications to figures. Revised protection language.
11/04	D	Corrected Table 4.
3/05	E	General corrections/reformatting.
3/07	F	Added notes regarding Power Supply Design Recommendations.
9/07	G	Removed dimensions from drawings and clarified notes on Erase, Write All, and Erase All commands. Updated protection language, identity guidelines.
11/30/07	H	Clarify SR4210PCB pin out to entire SR4000 receptacle family.
3/14/14	I	Updated Datakey logo.

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223-0017-003 REV I 3/14