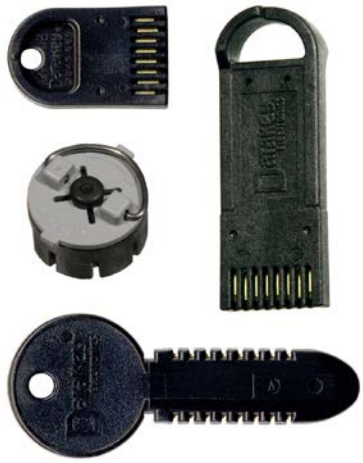
Datakey®

The power of memory. Secured.

SPI EEPROM
INTERFACE SPECIFICATION



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Notices and other considerations

Important notices

- Datakey guarantees the quality of its devices by testing each device before shipment. However, installing and using Datakey products is the responsibility of the purchaser and is in no way guaranteed by Datakey.
- Timing data, electrical characteristics, and signal descriptions are based on a compilation of several approved manufacturers' specifications. Datakey reviews the specifications of all approved vendors and "de-rates" the specifications as needed to ensure that all devices meet our published specifications regardless of the vendor used. Customers must design to our published specifications to ensure that all devices operate correctly within an application. Designing to a particular vendor's specifications is not recommended.
- **Design Recommendation:** It is recommended that all new key/token implementations be designed to operate with power supplies in the range of 2.7 to 3.6 volts. Although there is no immediate or certain future difficulties in the procurement of memory devices that operate with V_{cc} in the 4.5 to 5.5 volt range, it is possible the future availability of such memories may be impacted as semiconductor manufacturers continue to shrink their die geometries. Please contact the factory if you have any questions pertaining to this with your current or legacy design.
- While the information in this specification has been carefully reviewed, Datakey assumes no liability for any errors or omissions in this specification. Additionally, Datakey reserves the right to make changes to any part of the information in this specification or the products described herein without further notice.
- No part of this specification may be photocopied, reproduced, or translated to another language without the written consent of Datakey.

Other considerations

- Although portable keys and tokens are designed to withstand harsh environments, many of the conditions that prevent them from working properly in such environments are best addressed through properly designed system interface circuits.
- Datakey tests all keys and tokens during the manufacturing process. In some cases, data written to a keys or tokens remains after the test. Users should not rely on this data as a means of identifying keys/tokens.

Introduction

General description

Datakey portable memory keys and tokens contain electrically erasable programmable memory (EEPROM) accessed through a serial bus interface, using the Microwire, I²C, or SPI bus protocol. Each protocol controls input and output pins of the device through separate serial interface formats.

Portable memory device uses

Portable memory devices add functional versatility to many applications. They personalize equipment operations and transfer data in the following applications:

- Access control devices
- Instrument calibration equipment
- Fuel dispensers
- Medical treatment systems

Memory device design criteria

Portable memory applications require memory devices that can survive outside traditional environments, while maintaining data integrity when inserted and removed from the hosts powering them. Therefore, all portable memory devices must comply to the following basic design criteria:

- Resist dirt and other contaminants
- Transfer data reliably
- Tolerate electrostatic discharge
- Retain data when power is removed
- Retain data when exposed to certain environmental hazards

Manufacturers' design responsibility

Portable memory device manufacturers must address the above basic design criteria because they must develop memory devices capable of surviving in harsh environments. When a memory device is integrated into a larger system, the following design considerations become important:

- How to dissipate electrostatic discharge (ESD)
- How to maintain device data integrity
- How to prevent host system disruptions when inserting and removing a key or token

Continued on next page

Introduction, continued

Datakey portable memory devices

Datakey designs and manufactures portable, rugged keys and tokens containing non-volatile memory. Since 1976 our tough, reliable, and re-programmable keys, tokens, receptacles, and systems have solved data transport and access control problems in the most extreme environments.

Our SPI keys and tokens contain serial EEPROMs accessed through a simple three-wire or four-wire serial interface. Six simple instructions control data transfers to and from the SPI serial EEPROM. The Read instruction is used to access data stored in the device. The Write instruction stores data in the device.

All SPI serial EEPROM devices will power up in the Write disable state when V_{CC} *(supply voltage)* is applied.

What's in this specification

The remaining pages in this specification discuss SPI design criteria for portable memory devices and recommend ways to handle them in typical applications.

Functional description

Keys/Tokens

Figure 1 shows examples of serial EEPROM devices available from Datakey. Each type of key/token easily mates to a custom receptacle that provides access to SPI communication, power, and ground signals.

SSK SST SSX SSP

Figure 1: Serial EEPROM Devices

Signals

Table 1 presents KC4210 and SR4210 receptacles signal acronyms and descriptions. Communication between the microcontroller and devices on an SPI bus uses four signals:

Active low Chip Select (/CS)

Serial Clock (SCK)

Serial Data In (SI)

Serial Data Out (SO)

These signals, along with the V_{CC} *(supply voltage)* and ground signals are present on all keys/tokens.

Table 1: KC4210 and SR4210 Signal Acronyms and Descriptions

Signal Acronym	Signal Description
/CS	Chip Select Input
SI	Serial Data Input
SO	Serial Data Output
SCK	Serial Clock
/HOLD	Hold Serial Communication
V_{CC}	Supply Voltage
V_{SS}	Ground

Continued on next page

Functional Description (cont.)

Chip Select (/CS)

The /CS signal is an active low input to the device. A low level selects the device. A high level deselects the device and forces standby mode. However, an in-process programming cycle will be completed regardless of the state of the /CS input signal. If the /CS signal is driven high during a program cycle, the device will enter standby mode as soon as the programming cycle is completed. The /CS signal must be high for a short time specified by the t_{CS} *(chip select high)* between consecutive instructions. When the /CS signal is high, the internal control logic is held in a RESET status and all signal activity on SCK, SI and SO lines is ignored.

Serial Data Input (SI)

The SI signal is an input to the device. Information such as the opcode, address, and data bits are clocked into the device synchronously with the SCK input signal via the SI signal. Data latches in on the rising edge of the clock signal.

Serial Data Output (SO)

The SO signal is an output from the device; it is used in read mode to output data synchronously with the clock signal. It also provides /READY status information during write cycles.

Serial clock (SCK)

The SCK signal is used to synchronize the communication between the master device and the memory chip. Opcode, address, and data bits are clocked in on the rising edge of the SCK signal. Data bits are clocked out on the falling edge of the SCK signal. You can terminate the SCK signal anywhere in the transmission sequence *(at a HIGH or LOW level)* and it can be restarted anytime with respect to clock HIGH or clock LOW time. This gives the controlling master freedom to prepare the opcode, address, and data.

Hold (/Hold)

The /HOLD signal is used in conjunction with the /CS signal to pause serial communications with the Key/Token without resetting the clocking sequence:

To pause serial communications, assert the /HOLD signal while the SCK pin is low.

To resume serial communications, drive the /HOLD pin high while the SCK signal is low.

Inputs to the Serial Input pin (SI) are ignored while the SO signal is in a high-impedance state.

Continued on next page

Functional Description (cont.)

Supply voltage (V_{CC})

Our SPI keys and tokens will operate over a V_{CC} range of 2.7 – 5.5 volts. (See note at beginning of "Electrical Interface" Section.) **The supply voltage must be controlled so that keys and tokens are not inserted into live receptacles. See section entitled "Memory Device Power and Signal Control".**

Ground (GND)

The ground signal and the system ground signal are common.

SPI Modes

Our SPI keys and tokens support SPI modes "0" (0,0) and "3" (1,1). All timing diagrams and instruction descriptions assume mode "0" operation.

Status register

The status register contains a number of status and control bits that can be read or set as needed by specific instructions—the format is shown in Table 2.

Table 2: Status Register Control and Status Bit Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	/RDY

/RDY bit: The /READY bit indicates whether the memory is busy with a write or write status register cycle. Bit 0 = "0" indicates a write cycle is not in progress.

WEN bit: The write enable latch bit indicates the status of the internal write enable latch.

BP1, BP0 bits: Block write protection is enabled by programming the status register with one of four blocks of write protection. The block protect *(BP1, BP0)* bits are non-volatile. They define the size of the area to be software protected against Write instructions. Table 3 shows write-protected block sizes.

Table 3: Write-Protected Block Size

		Protected Block	Protected Addresses					
BP1	**BP0**		**2K bit**	**4K bit**	**8K bit**	**16K bit**	**64K bit**	**256K bit**
0	0	None	None	None	None	None	None	None
0	1	Upper quarter	C0-FF	180-1FF	300-3FF	600-7FF	1800-1FFF	6000-7FFF
1	0	Upper half	80-FF	100-1FF	200-3FF	400-7FF	1000-1FFF	4000-7FFF
1	1	Whole memory	00-FF	00-1FF	000-3FF	000-7FF	0000-1FFF	0000-7FFF

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Instructions

Read and write operations

SPI keys and tokens contain an eight-bit instruction register used to facilitate Read and Write operations. There are six instructions: Read, Write, Read Status Register, Write Status Register, Write Enable, and Write Disable. The format of each instruction is shown in Table 4.

Instructions, addresses, and input data bytes are shifted into the device most significant bit first. The Serial Data Input (SI) signal is sampled on the first rising edge of the Serial Clock (SCK) signal after the Chip Select (/CS) signal.

All output bytes are shifted out most significant bit first. The Serial Data Output (SO) is latched on the first falling edge of the SCK signal.

Instruction format

Each instruction follows the same basic format and contains the following information.

Opcode bits: The opcode byte is the first byte following the /CS assertion. The opcode specifies the operations to perform.

Address bits: Address bits follow the opcode bits. The number of address bits clocked in depends on the capacity of the device being addressed. As described previously, some instructions use the first two bits of the address field. For those instructions, it is still necessary to clock in the correct number of address bits *(including the first two bits*) for the device being addressed; however, the bits are DON'T CARE values.

Data bits: The data bits for instructions with a data field associated with them *(Read/Write)* follow the address bit field. The data bits are clocked in on the data in (SI) signal for a Write instruction. The data bits are clocked out from the data out (SO) signal for a Read instruction.

Continued on next page

Instructions, continued

Instruction set

The serial instructions for all SPI keys and tokens differ only in the length of the address required. The smaller keys and tokens *(2Kbit and 4Kbit)* use the most significant bit of the lower nibble of the eight-bit instruction code as the most significant address bit.

Table 4 shows the instruction set.

Table 4: Instructions Sets

Acronym	Format	Description
	bit_7 - bit_0	
WREN	0000 0110	Set write enable latch *(enable Write operations)*
WRDI	0000 0100	Reset write enable latch *(disable writes)*
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register
READ	0000 0011	Read data from memory starting at selected address
WRITE	0000 0010	Write data to memory beginning at selected address

Note: Bit "3" is used as the most significant address bit for 4Kbit keys or tokens.

SPI device read and write cycles

Read cycles

First, the Chip Select (/CS) signal is driven low. Then the instruction and address bits are shifted in on the Serial Data Input (SI) pin. The address bits load into an internal address register, and the data byte at that address is shifted out on the serial data output (SO) pin.

Sequential reads can be performed by keeping the /CS signal low. This causes the internal address register to automatically increment, and the data byte at the new address to shift out. When the highest address is reached, the address counter rolls over to zero, allowing the read cycle to continue indefinitely.

The whole memory can therefore be read with a single Read instruction. The read cycle is terminated by driving the /CS signal high. The rising edge of the /CS signal can occur at any time during the read cycle. The first byte addressed can be any byte within any page. The instruction is neither accepted nor executed during a write cycle. See Figure 2 for read cycle timing.

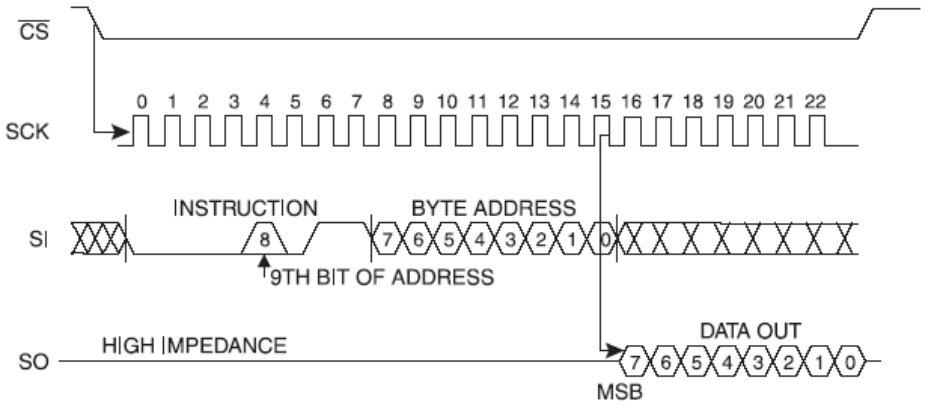

Figure 2: Read Cycle Timing Chart

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SPI device read and write cycles, continued

Write enable/ disable

When power is applied to a key or token, the device enters the programming disabled state; therefore, a Write Enable (WREN) instruction must precede the Write instruction. See Figures 3 and 4 for Write Enable and Disable timing. Read instructions are not affected by the programming state of the device.

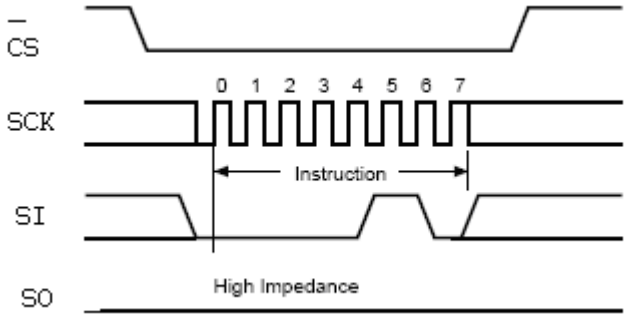

Figure 3: Write Enable Timing Chart

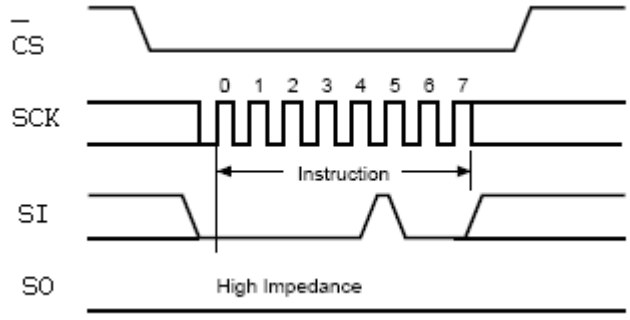

Figure 4: Write Disable Timing Chart

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SPI device read and write cycles, continued

Write cycles

The device must be Write Enabled via the WREN instruction before executing a Write instruction. First, the Chip Select (/CS) signal is driven low. Then the instruction and address bits, address byte and at least one data byte shift in on the Serial Data Input (SI) pin. The instruction is terminated by driving the /CS signal high at a byte boundary of the input data. If this occurs after the eighth bit of the data byte has been latched in, the instruction is being used to Write a single byte. See Figures 5 and 6.

If the /CS signal continues to be driven low, the next data byte shifts in so that more than a single byte, starting from the given address towards the end of the same page, can be written in one internal write cycle. Each time a new data byte shifts in, the least significant bits of the internal-address counter increment. See Figure 6. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the start of the page and the existing data is overwritten with the incoming data. See Figure 7.

Table 5 shows the page size of various keys and tokens.

Table 5: Page Size

Key/Token Capacity	2Kbit	4Kbit	8Kbit	16Kbit	64Kbit	256Kbit
Pages	32	64	16	64	256	512
Page Size *(bytes)**	8	8	16	32	32	64

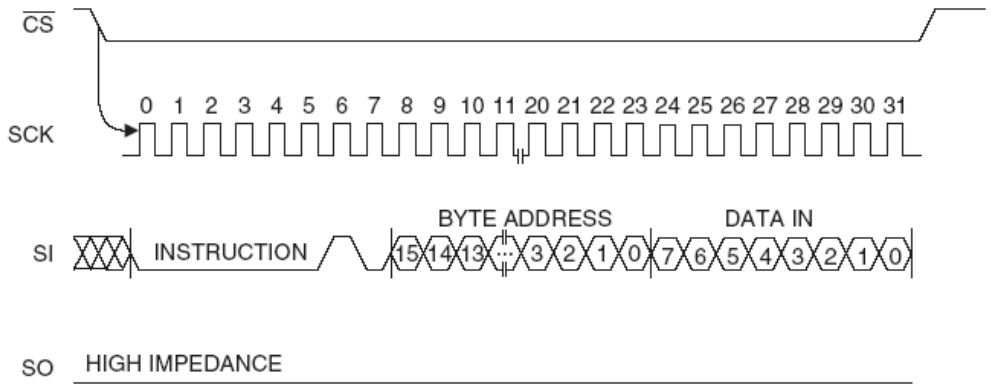

Figure 5: Byte Write Cycle Timing Chart

* It is recommended that all new key/token implementations not rely on specified page size for achieving a wrap-around effect for the effective memory address. Although Datakey has no intention to deviate from the listed specification, some semiconductor manufacturers offer devices with page sizes that differ from those published here. We feel a good engineering practice would be to not rely on the listed value in the event availability becomes an issue in the future. The page size in our memory products will be at least as large as what is specified here.

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SPI device read and write cycles, continued

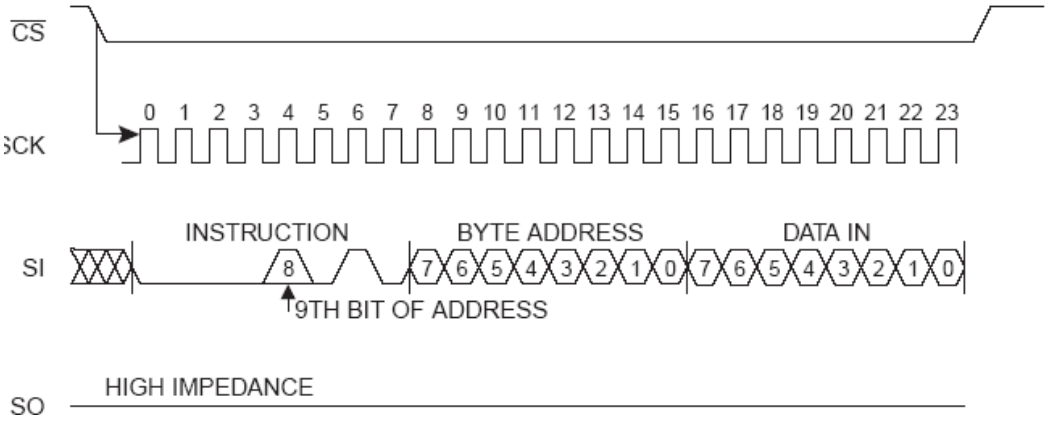

Figure 6: Byte Write Cycle Timing Chart (4Kbit)

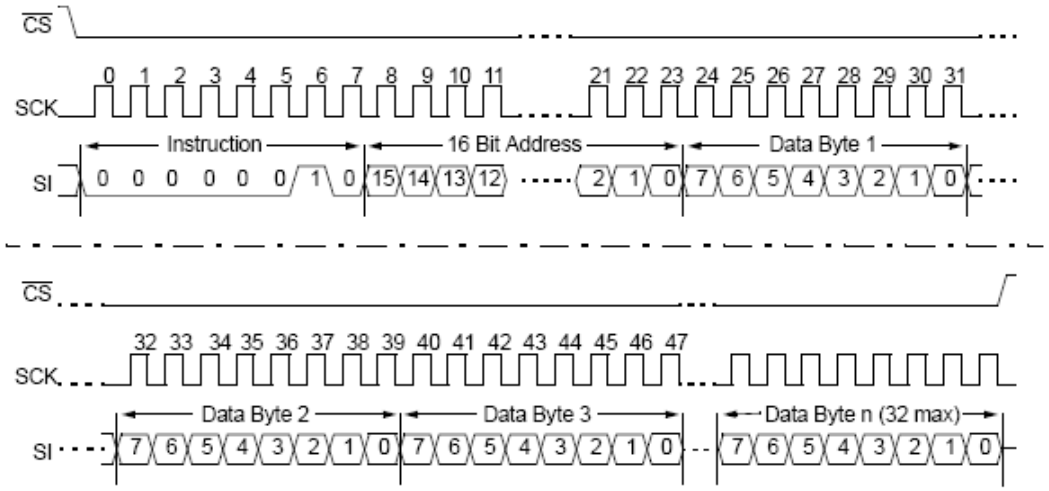

Figure 7: Page Write Cycle Timing Chart

Continued on next page

SPI device read and write cycles, continued

Write status register

The Write Status Register (WRSR) instruction allows selecting one of four protection levels. The devices are divided into four array segments—one quarter (1/4), one half (1/2) or all memory segments can be protected. Any data within a selected segment will therefore be READ only. See Figure 8 for Write Status Register Instruction Timing. The block-write protection levels and corresponding status register control bits are shown in Table 3. The two bits, BP0 and BP1 are nonvolatile cells that have the same properties and function as regular memory cells.

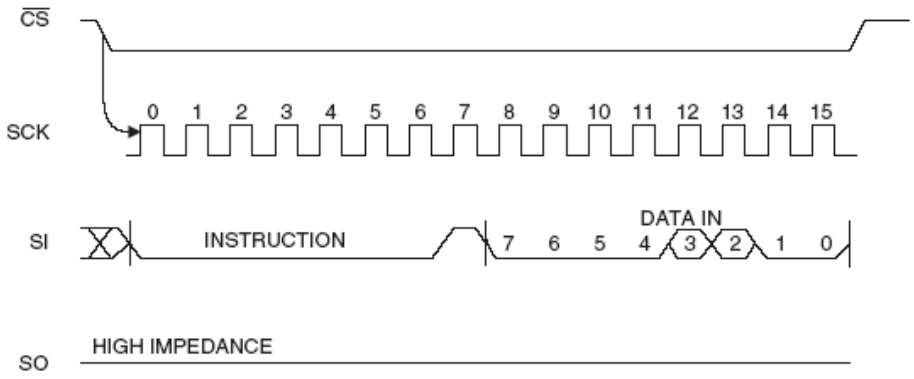

Figure 8: Write Status Register Instruction Timing

Read status register

The Read Status Register (RDSR) instruction provides access to the status register. The READY/BUSY and write enable status of the device can be determined by the RDSR instruction. Similarly, the block-write protection bits indicate the extent of the protection employed. These bits are set by using the WRSR instruction. See Figure 9 for Read Status Register Instruction Timing.

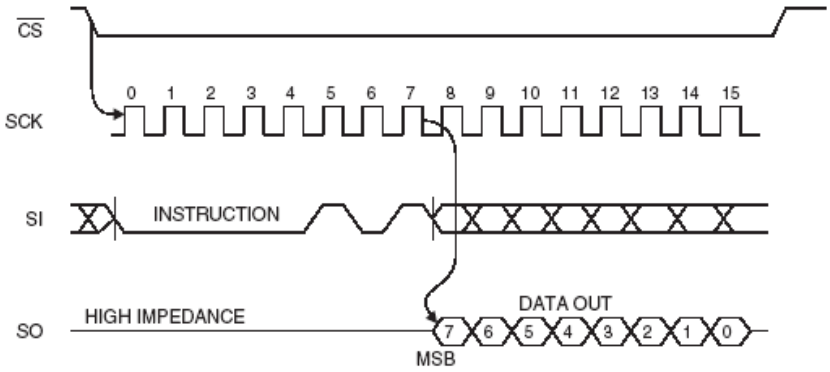

Figure 9: Read Status Register Instruction Timing

Panel/board-mount receptacle descriptions

Receptacles

The receptacles are used to interface the host system directly with specific serial data keys/tokens. The types are the KC4210, KC4210PCB, SR4210, and the SR4210PCB.

A Last On/First Off (LOFO) switch in the key or token receptacle enables the host system to determine when a key or token is present. Upon insertion of a key or token, the LOFO contact connects to ground. Conversely, when the key is removed, the LOFO contact is open. The LOFO contact allows system designers to detect the presence of a key or token, and protects the host bus by applying power only when a key or token is fully inserted into the receptacle.

KC4210 panel-mount receptacle

The KC4210 panel-mount version is designed for an application that requires easy mounting in a front-panel configuration. To mount the receptacle, simply cut a one-inch square hole in the desired panel location and then snap the receptacle into place. Figure 10 show a picture of the receptacle. A standard 10-pin connector cable *(5 x 2)* is used to connect the device to the host.

Figure 10: KC4210 Panel-Mount Receptacle

Note: It is recommended that the total length of signal conductors, PC board traces, and ribbon cables not exceed eight inches.

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Panel/board-mount receptacle descriptions, continued

KC4210 orthographic drawing

Figure 11 shows the KC4210 panel-mount receptacle. Refer to spec sheet for dimensions.

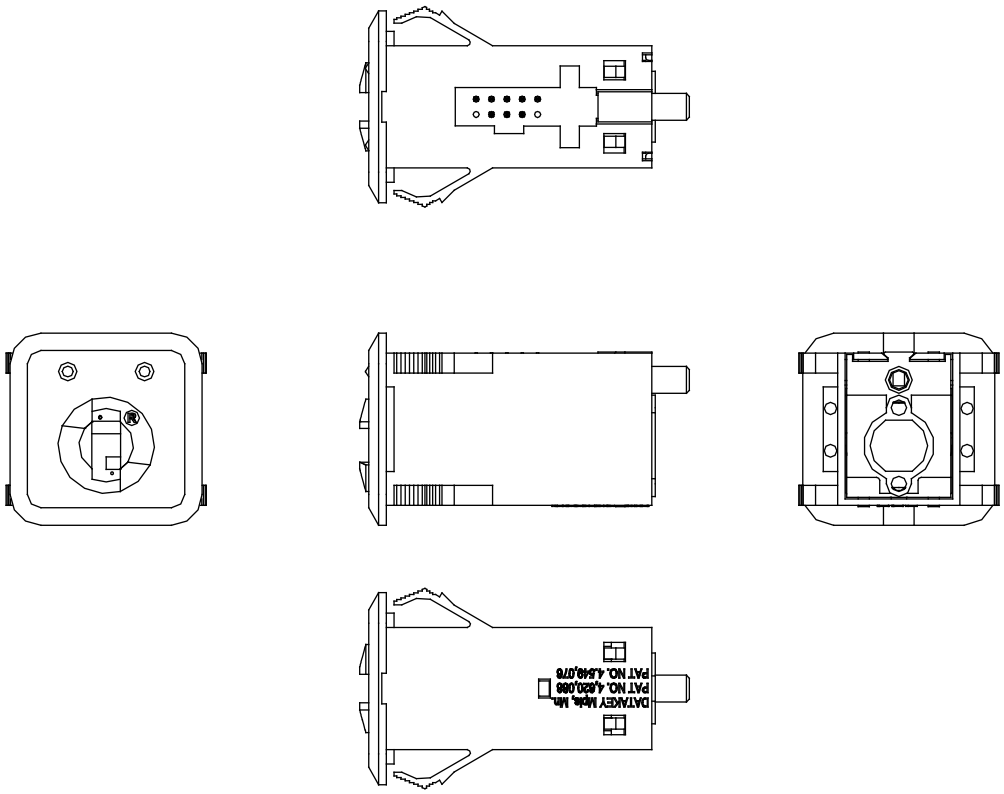

Figure 11: KC4210 Panel-Mount Receptacle Orthographic Drawing

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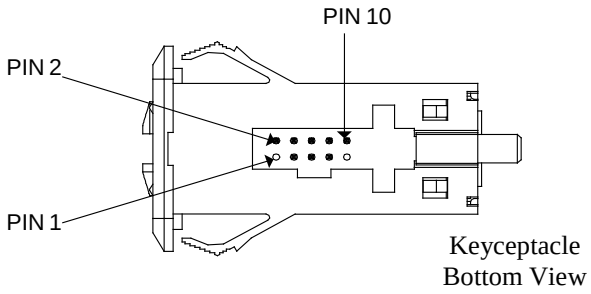
Panel/board-mount receptacle descriptions, continued

KC4210 pin outs

Figure 12 shows KC4210 receptacle pin outs.



SPI	
Pin No.	**Description**
Pin 1	NC
Pin 2	Power (V_{CC})
Pin 3	Ground (V_{SS})
Pin 4	/Hold
Pin 5	Chip Select (/CS)
Pin 6	Data In (SI)
Pin 7	Serial Clock (SCK)
Pin 8	Data Out (SO)
Pin 9	NC
Pin 10	LOFO

Figure 12: KC4210 Receptacle Pin Outs

Continued on next page

Panel/board-mount receptacle descriptions, continued

KC4210PCB mount receptacle

The KC4210PCB receptacle is designed for applications where the designer wants to mount the device directly onto a printed circuit board (PCB). In such applications, the PCB-mount receptacle can be connected to the host by soldering its leads onto a printed circuit board. Figure 13 shows a picture of the receptacle.

Figure 13: KC4210PCB Mount Receptacle

KC4210PCB orthographic drawing

Figure 14 shows the KC4210PCB mount receptacle. Refer to the spec sheet for dimensions.

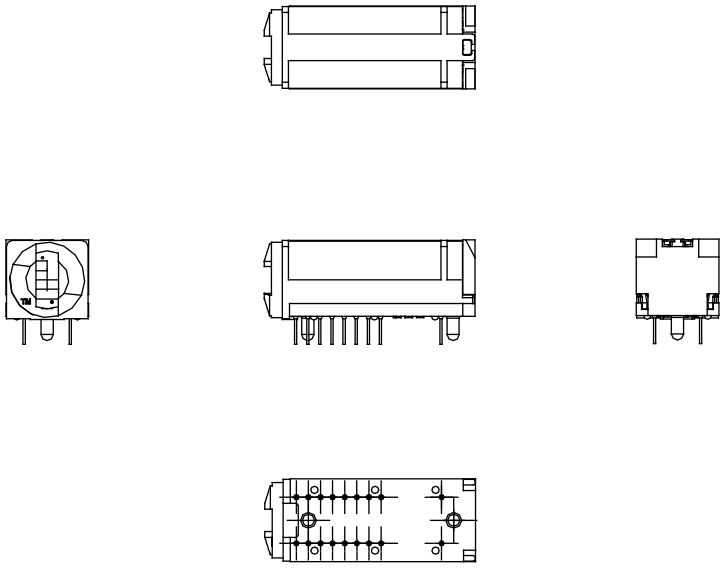


Figure 14: KC4210PCB Receptacle Orthographic Drawing

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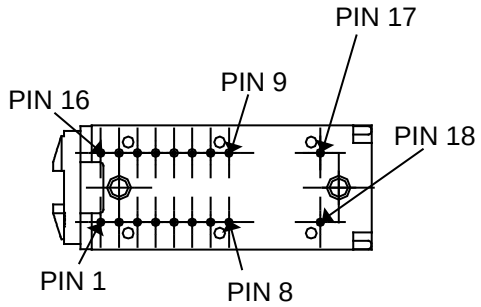
Panel/board-mount receptacle descriptions, continued

KC4210PCB pin outs

Figure 15 shows receptacle pin outs.



Receptacle
Bottom View

SPI	
Pin No.	**Description**
Pin 1	/Hold
Pin 2	Ground (V_{SS})
Pin 3	Power (V_{CC})
Pin 4	NC
Pin 5	Data Out (SO)
Pin 6	Chip Select (/CS)
Pin 7	Serial Clock (SCK)
Pin 8	Data In (SI)
Pin 9	Data In (SI)
Pin 10	Serial Clock (SCK)
Pin 11	Chip Select (/CS)
Pin 12	Data Out (SO)
Pin 13	NC
Pin 14	Power (V_{CC})
Pin 15	Ground (V_{SS})
Pin 16	/Hold
Pin 17	LOFO
Pin 18	LOFO

Figure 15: KC4210PCB Receptacle Pin Outs

KC4210 key style & pin outs

The KC4210 panel- and board-mount receptacles accept the SSK style key. See Figure 16.

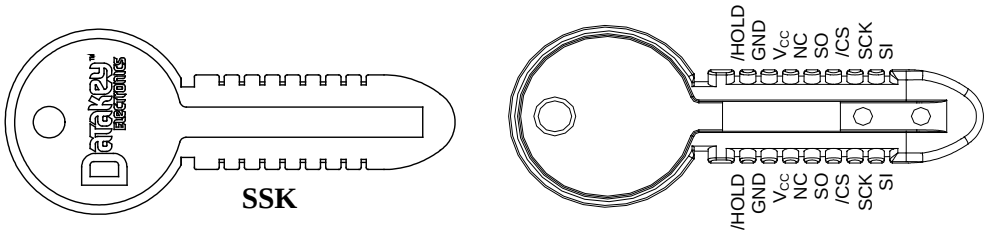


Figure 16: SSK Keys for KC4210 Receptacle and Key Pin Out

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Panel/board-mount receptacle descriptions, continued

SR4210 panel-mount receptacle

The SR4210 panel-mount version is designed for applications that require easy mounting in a front-panel configuration. To mount the SR4210 panel-mount receptacle, simply cut a hole based on the dimensions shown on the SR4210 spec sheet in the desired panel location and then snap it into place. A standard 10-pin connector cable *(5 x 2)* is used to connect the device to the host. A Last On/First Off (LOFO) switch in the receptacle enables the host system to determine when a token is present. Figure 17 shows a picture of the receptacle.

Figure 17: SR4210 Panel-Mount Receptacle and Clip

Note: It is recommended that the total length of signal conductors, PC board traces, and ribbon cables not exceed eight inches.

SR4210 orthographic drawing

Figure 18 shows the SR4210 panel-mount receptacle. Refer to the spec sheet for dimensions.

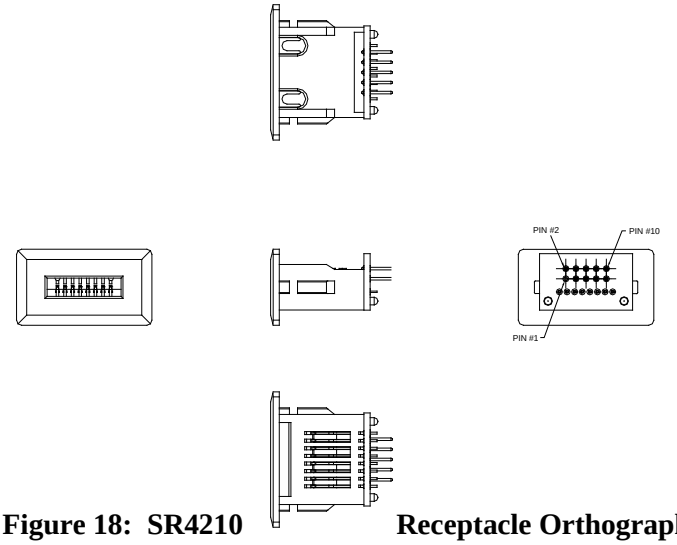

Figure 18: SR4210 Receptacle Orthographic Drawing

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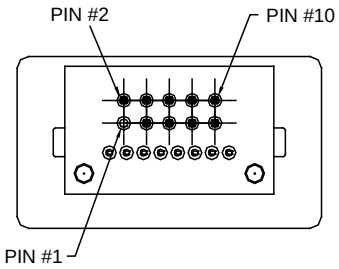
Panel/board-mount receptacle descriptions, continued

SR4210 pin outs

See Figure 19 for receptacle pin outs.



SPI	
Pin	**Description**
Pin 1	NC
Pin 2	Power (V_{CC})
Pin 3	Ground (V_{SS})
Pin 4	NC
Pin 5	Chip Select (/CS)
Pin 6	Data In (SI)
Pin 7	Serial Clock (SCK)
Pin 8	Data Out (SO)
Pin 9	/Hold
Pin 10	LOFO

Figure 19: SR4210 Receptacle Pin Outs

SR42XXPCB mount receptacles

The information on the SR4210PCB below also applies to the SR4220, SR4230 board-mount receptacles. Dimensions can be found in the corresponding spec sheets. Contact the factory for information on SMT options.

SR4210PCB mount receptacle

The SR4210PCB mount receptacle is designed for applications where the designer wants to mount the receptacle directly onto a printed circuit board (PCB). In such applications, the receptacle can be mounted to the host by soldering its leads onto a printed circuit board. Figure 20 shows a picture of the receptacle.

Figure 20: SR4210PCB Mount Receptacle

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Panel/board-mount receptacle descriptions, continued

SR4210PCB orthographic drawing

Figure 21 shows the SR4210PCB mount receptacle. Refer to the spec sheet for dimensions.

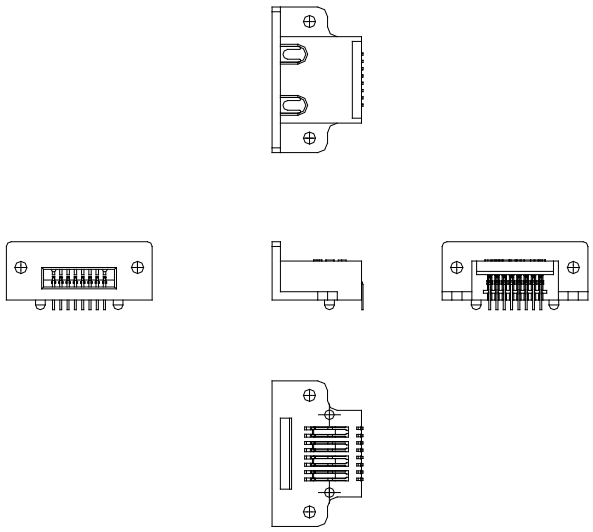
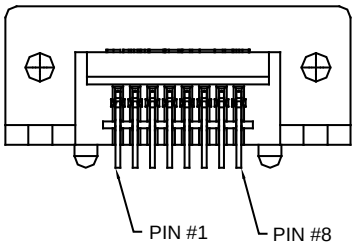


Figure 21: SR4210PCB Mount Receptacle Orthographic Drawing

SR4210PCB pin outs

See Figure 22 for SR4210PCB mount receptacle pin outs.



SPI	
Pin	**Description**
Pin 1	/Hold
Pin 2	Power (V_{CC})
Pin 3	Chip Select (/CS)
Pin 4	Serial Clock (SCK)
Pin 5	Data In (SI)
Pin 6	Data Out (SO)
Pin 7	Ground (V_{SS})
Pin 8	LOFO

Figure 22: SR4210PCB Mount Receptacle Pin Outs

Continued on next page

Panel/board-mount receptacle descriptions, continued

Slim token styles & pin outs

The SR4210 panel- and PCB-mount Receptacles accept the SST tokens and SSX extended tokens, with memory sizes from 2Kb to 256Kb. See Figure 23 for token styles and pin out. **Note:** The tokens have redundant contacts. Pin out shown applies to both views of the token.

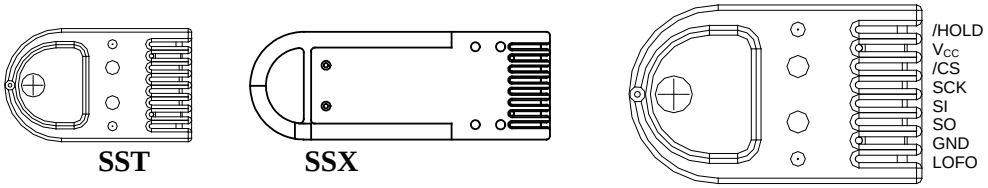


Figure 23: SST Token / SSX Extended Token Styles and Pin Out

KSD receptacle

The KSD receptacle accepts SSP plugs. It can be used in board- and panel-mount applications. Figure 24 and 25 show pictures of the KSD receptacle and SSP plug.

Figure 24: KSD Receptacle

Figure 25: SSP Plug

Continued on next page

Panel/board-mount receptacle descriptions, continued

KSD receptacle orthographic drawing

Figure 26 shows the KSD board-mount receptacle. Refer to spec sheet for dimensions.

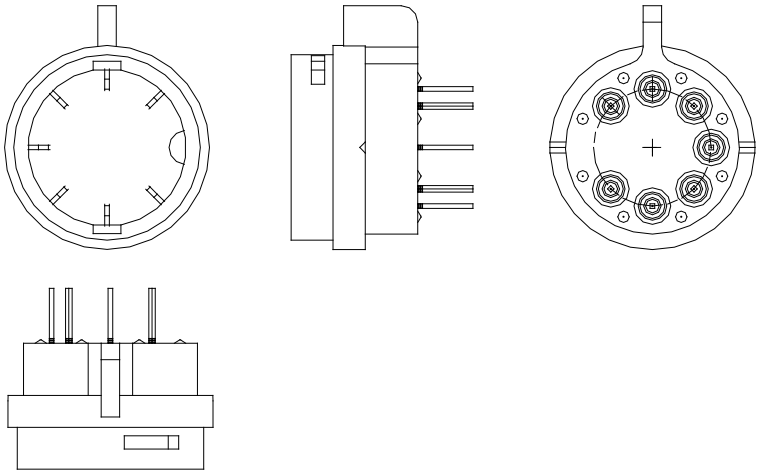
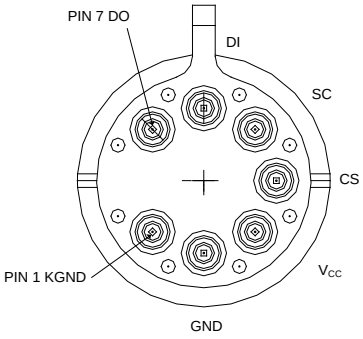


Figure 26: KSD Receptacle Orthographic Drawing

KSD/SSP pin outs

Figure 27 shows a bottom view of a KSD receptacle diagram and a description of its pin outs when used with an SSP plug.



SPI	
Pin	**Description**
Pin 1	KGND*
Pin 2	Ground
Pin 3	Power (VCC)
Pin 4	/Chip Select
Pin 5	Serial Clock
Pin 6	Serial Data In
Pin 7	Serial Data Out

***Note:** KGND is connected to GND inside the plug. When a plug is inserted into the receptacle, the host monitors the KGND signal to determine the presence of the plug. KGND is pulled "low."

Figure 27: KSD/SSP Receptacle Pin-Out Positions and Description

Electrical interface

Electrical characteristics

Tables “6” thru “8” show specific common DC and AC electrical characteristics for serial SPI EEPROM Keys and Tokens.

Caution

The conditions shown in Table “6” are stress ratings only. Stressing SPI keys and tokens beyond the maximum limits specified in Tables “6” thru “8” could compromise performance or cause permanent damage to keys and tokens.

Table 6: Absolute Maximum Values and Temperatures

Symbol	Parameter	Min/Max	Units
V_{CC}	Supply voltage	6.25	V
$V_{IN/OUT}$	All pins w.r.t. Ground	-0.5 to 6.5	V
T_{STG}	Storage temperature	-65 to 150	°C
T_{BIAS}	Operating temperature[1]	-40 to 85	°C

[1] Keys and tokens manufactured before 2004 have an operating temperature range of 0°C to 70°C.

Design Recommendation: It is recommended that all new key/token implementations be designed to operate with power supplies in the range of 2.7 to 3.6 volts. Although there is no immediate or certain future difficulties in the procurement of memory devices that operate with V_{cc} in the 4.5 to 5.5 volt range, it is possible the future availability of such memories may be impacted as semiconductor manufacturers continue to shrink their die geometries. Please contact the factory if you have any questions pertaining to this with your current or legacy design.

Continued on next page

Electrical interface, continued

Table 7: DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Supply voltage	2.7	5.5	V	5.0 V nominal
V_{IH}	High level voltage input	0.7xVcc	Vcc + 0.5	V	
V_{IL}	Low level voltage input	-0.3	0.3xVcc	V	
V_{OH}	High level voltage output	.8xVcc		V	I_{OL} = -0.4mA, Vcc =2.5 V
V_{OL}	Low level voltage output		0.4	V	I_{OL} = 2.1 mA, Vcc = 4.5 V
I_{LI}	Input leakage current		± 2.0	µA	V_{IN} = 0 to Vcc
I_{LO}	Output leakage current		± 3.0	µA	/CS = Vcc
C_{IN}	Input pin capacitance		8.0	pF	V_{IN} = 0 V
C_{OUT}	Output pin capacitance		8.0	pF	V_{OUT} = 0 V
I_{CC}	Supply current		7.0	mA	SO = open, SCK =1 MHz, Vcc = 5.0 V
I_{CCS}	Supply current standby		3.0	µA	Vcc = 2.7V, /CS = Vcc

Electrical interface, continued

Table 8: AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
f_{SK}	Clock frequency		5	MHz
t_{SKH}	Clock high time[1]	100		ns
t_{SKL}	Clock low time[1]	100		ns
t_{SKS}	Clock setup time	200		ns
t_{CSS}	Chip select setup time	200		ns
t_{CSH}	Chip select hold time	200		ns
t_{CS}	Chip select high[2]	200		ns
t_{DIS}	Data in setup time	50		ns
t_{DIH}	Data in hold time	50		ns
t_{PDV}	Delay to output valid		40	ns
t_{LZ}	/Hold high to output low Z		100	ns
t_{HZ}	/Hold low to output high Z		250	ns
t_{WC}	Write cycle time		10	ms

Notes:

1. $t_{SKH} + t_{SKL} \geq 1/f_{SK}$
2. The Chip Select signal must be brought high for a minimum of t_{CS} between consecutive instructions.

Timing diagrams

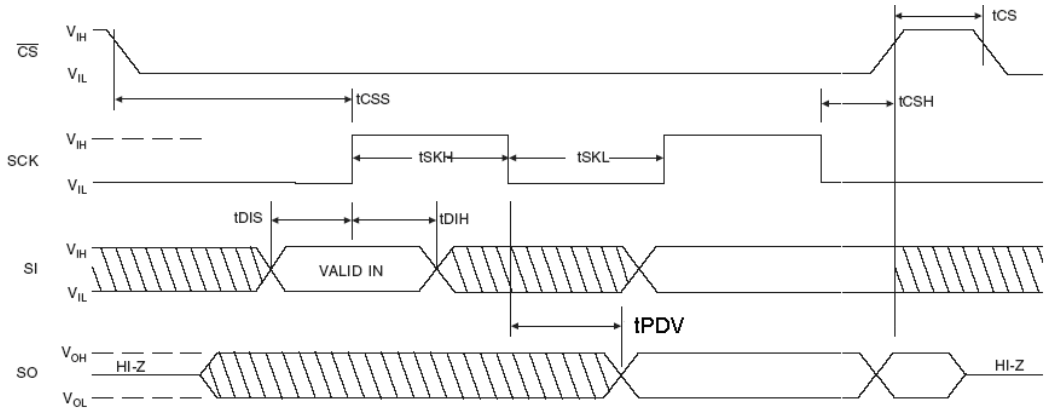


Figure 28: Synchronous Data Timing

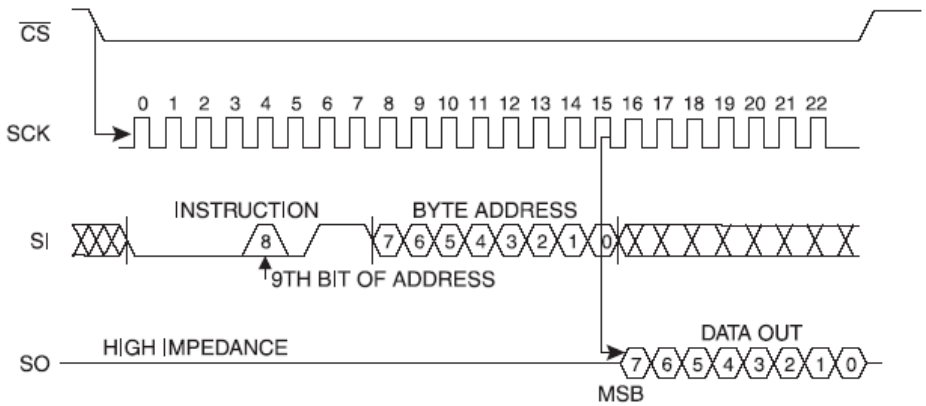


Figure 29: Read Operation Timing (2Kbit, 4Kbit)

Continued on next page

Timing diagrams, continued

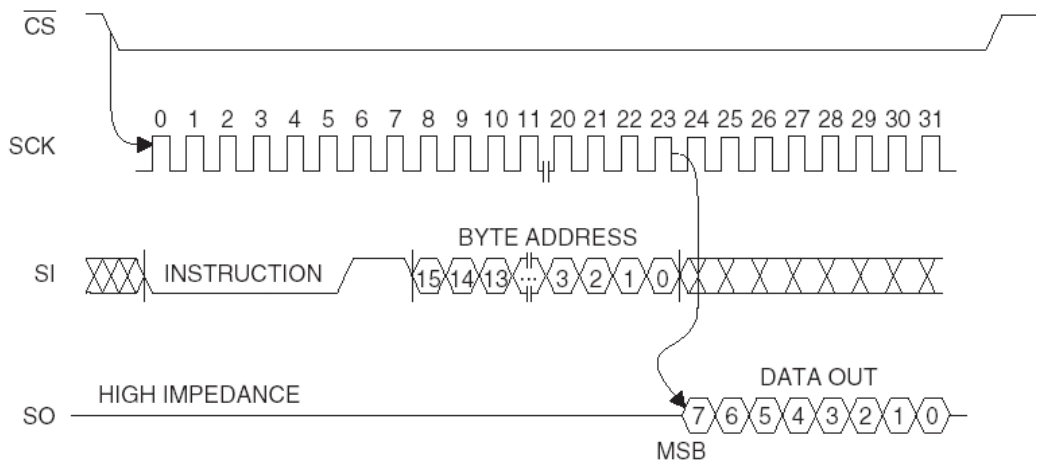


Figure 30: Read Operation Timing (memory densities > 4Kbits)

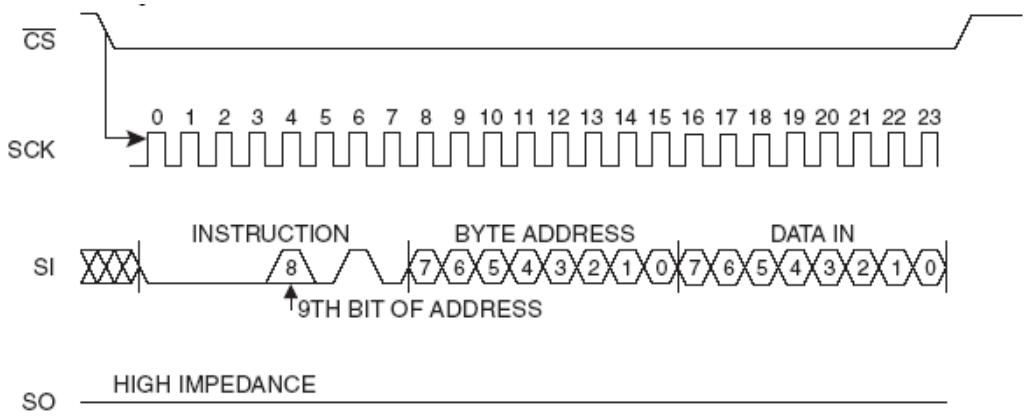


Figure 31: Write Operation Timing (2Kbit, 4Kbit)

Continued on next page

Timing diagrams, continued

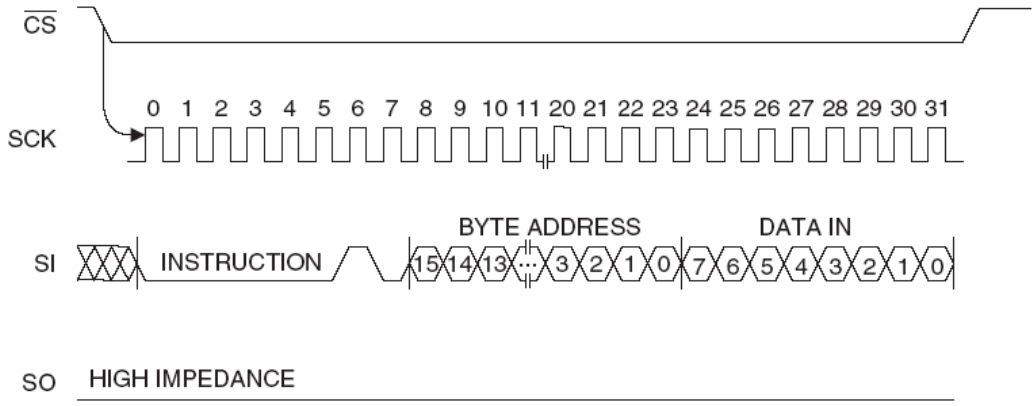


Figure 32: Write Operation Timing (memory densities > 4Kbits)

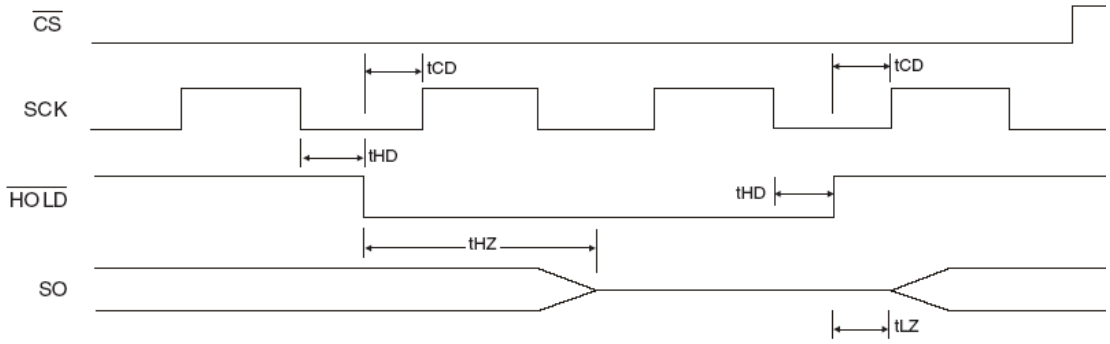


Figure 33: /HOLD Timing

Electrostatic discharge (ESD)

Circuit component damage

A buildup of electrostatic charge gradients across the surface of a memory device can produce voltages that could damage circuit components. To prevent such damage, Datakey portable memory devices integrate materials, circuits, and mechanical barriers that help to ensure uniform voltage across the circuit.

Electrostatic charge voltage levels

Any system that uses memory devices must also provide a means of dissipating electrostatic charges. By simply holding a portable memory device in your hand, it is possible to build up an electrostatic charge across the surface of the memory device up to 20KV relative to ground. This would be equivalent to connecting a circuit of several hundred picofarads of capacitance with a low-series resistance to the memory device.

Electrostatic charge dissipation

When you insert a portable memory device into a system that is grounded or at some other potential, the built-up charge from handling the memory device must be safely dissipated. This can be done by providing a path to ground for the charge. The path must be controlled to prevent large currents and high voltages from occurring on the memory device and in the receptacle. This can be done by putting a resistor in the circuit trace for the receptacle, and using over-voltage protection devices to direct the charge to system ground.

Memory device power and signal control

Poor contact concerns

When inserting a portable memory device into a receptacle, there can be poor contact between the memory device and the receptacle. There could be several possible causes:

Dirty contact surfaces: To make enough electrical contact, the contact surfaces must be free of contaminants. This requires that the contacts be cleaned through a wiping action from the portable memory device.

The contacts could bounce and require some time to settle. This could result in a series of random make and break conditions on any or all the contacts.

When a memory device is removed from a receptacle, the contacts do not always break evenly or cleanly.

Power concerns

When power is applied to a memory device when inserted or removed from a receptacle, random contact makes and breaks could cause significant problems for the memory device and the receptacle. Because the control and address signals are not controlled during those actions, undesirable logic combinations could occur, such as the following:

Power and ground connections becoming unstable, causing further unpredictability

Fast power switching to a memory device can introduce noise into system power and ground distribution circuits, resulting in electrical damage to the memory device and data corruption

Data corruption prevention

The integrated circuits used in Datakey keys and tokens are designed to reduce the risk of data corruption during transient conditions. For example, keys and tokens require a Write Enable instruction before storing any data. Write instructions are also not permitted if the supply voltage is less than a prescribed value. As effective as these protection schemes might be, they do not always eliminate the potential problems with noise that could occur when power is applied to a circuit via a bouncing contact.

To avoid these problems, it is important to control the key and token's power and signal connections. This can be done by using detection circuits, which are discussed next.

Continued on next page

Memory device power and signal control, continued

Memory device detection circuit

The memory device detection circuit detects when a memory device is present. Datakey receptacle uses Last On/First Off (LOFO) contacts for this purpose. When inserting a memory device into the receptacle, the LOFO contacts make electrical connection only after all memory device contacts are closed. Similarly, the LOFO contacts break before any other contact is open.

Transistor switch circuit

When a receptacle detects a memory device for a certain minimum time, power can then be applied. This delay can be established by using a simple transistor switch circuit with the following characteristics:

The power switch should have a low voltage drop when power is applied to the memory device. This will ensure that the voltage supplied to the key/token is within a safe and acceptable range.

The circuit should apply power to any pull-up resistors connected to the key or token to prevent power from being applied unintentionally through the signal lines.

The circuit should include a bleeder resistor to ensure that power is removed quickly when the switch is turned OFF.

The switch should turn power ON fast enough to avoid causing problems in the key or token, and slow enough so that it does not introduce any significant noise into the system-reset circuit.

SPI read and write procedures

Procedures

Follow the procedures below when using a key or token in a receptacle with a power switching circuit.

Read procedure

The procedure for reading data from a key or token is less critical than the sequence for writing data to that same key or token because the data is not subject to change. To read the data from a key or token, Datakey recommends the following procedure:

Insert the key or token
Detect the key or token using the LOFO contact
Wait for contacts to settle (verify memory device is still present)
Apply power
Wait for power to stabilize
Test contact integrity
Read data
Remove power
Remove the key or token

Continued on next page

SPI read and write procedures (cont.)

Write procedure

The write procedure must verify that the key or token is present throughout the write cycle, which will ensure that data are written to the key or token correctly. To write data to a key or token, Datakey recommends the following procedure:

Insert the key or token
Detect the key or token using the LOFO contact
Wait for contacts to settle (verify key or token is still present)
Apply power
Wait for power to stabilize
Test contact integrity
Write data
Verify key or token is still present *(if not, indicate an error)*
Verify the data written (if appropriate, indicate an error)
Remove power
Remove the key or token

Long read/write operation

Large capacity memory systems should also be protected against key or token removal during long Read or Write operations. An activity light might be all that is needed for some applications. Other installations could require physical barriers or interlocks to ensure that the key or token being read or written to remains in place.

Acknowledgement

Atmel Corporation

Timing diagrams courtesy of Atmel Corporation.

Revision History

Date	Revision	Description
1/28/05	A	Initial issue of SPI EEPROM interface specification.
2/8/05	B	Corrections to signal and instruction descriptions. Corrections to Electrical Interface charts.
2/24/05	C	RDSR chart correction.
3/25/05	D	Reformatted to new template.
9/12/06	E	Corrected: Table 5 (8Kbit page Size); Table 7 (supply current SCK condition); Fig 25 (read timing chart). Updated with new logo and protection language.
3/15/07	F	Added notes regarding Power Supply Design Recommendation.
9/20/07	G	Removed dimensions from drawings. Added warning not to use page size wrap around to write cycle info, corrected Table 7 (I_{ol}, I_{cc} and SCK), corrected Table 8 (t_{skm} and t_{skl}); and updated for corporate identity.
11/29/07	H	Add SSP Plug information and clarify SR4210PCB pin out to entire SR4000 receptacle family.
3/14/14	I	Updated Datakey logos.

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